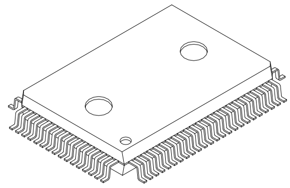
SONY

CXD2500BQ

CD Digital Signal Processor

80 pin QFP (Plastic)



Description

The CXD2500BQ is a digital signal processing LSI designed for use in compact disc players. It has the following functions:

- Wide-frame jitter margin (±28 frames) realized by a built-in 32K RAM.
- Bit clock generated by digital PLL for strobing EFM signals. Capture range of ±150 kHz and over.
- EFM data demodulation
- Enhanced protection of EFM Frame Sync signals
- Powerful error correction based on Refined Super Strategy
  Error correction C1: Double correction
  C2: Quadruple correction
- Double-speed playback and vari-pitch playback
- Reduced noise generation at track jump
- Auto zero-cross muting
- Subcode demodulation and subcode Q data error detection
- Digital spindle servo system (incorporating an oversampling filter)
- 16-bit traverse counter
- Built-in asymmetry correction circuit
- CPU interface using a serial bus
- Servo auto sequencer
- Output for digital audio interface
- Built-in digital level meter and peak meter
- Bilingual

Features

- All digital signals for regeneration are processed using one chip.
- The built-in RAM enables high-integration mounting.

Structure

Silicon-gate CMOS IC

Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	–0.3 to +7.0	V
• Input voltage	V_I	–0.3 to +7.0	V
• Output voltage	V_O	–0.3 to +7.0	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–40 to +125	°C
• Supply voltage differences	V_{SS}–AV_{SS}	–0.3 to +0.3	V
	V_{DD}–AV_{DD}	–0.3 to +0.3	V

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.75*1 to 5.25*3 (5.0 V typ.)	V
• Operating temperature	Topr	–20 to +75	°C
• Input voltage	V_{IN}	V_{SS}–0.3 to + V_{DD} + 0.3	V

*1 V_{DD} value of 4.75 V (min.) is for the double-speed playback mode at vari-pitch control reset. For the low power consumption special playback mode, V_{DD} value is 3.6 V (min.). *2 In the normal-speed playback mode V_{DD} value is 4.5 V (min.)

*2 Low power consumption, special playback mode
Set the internal operation of LSI at the double-speed mode, and half the crystal oscillation frequency. This will result in the normal-speed playback mode.

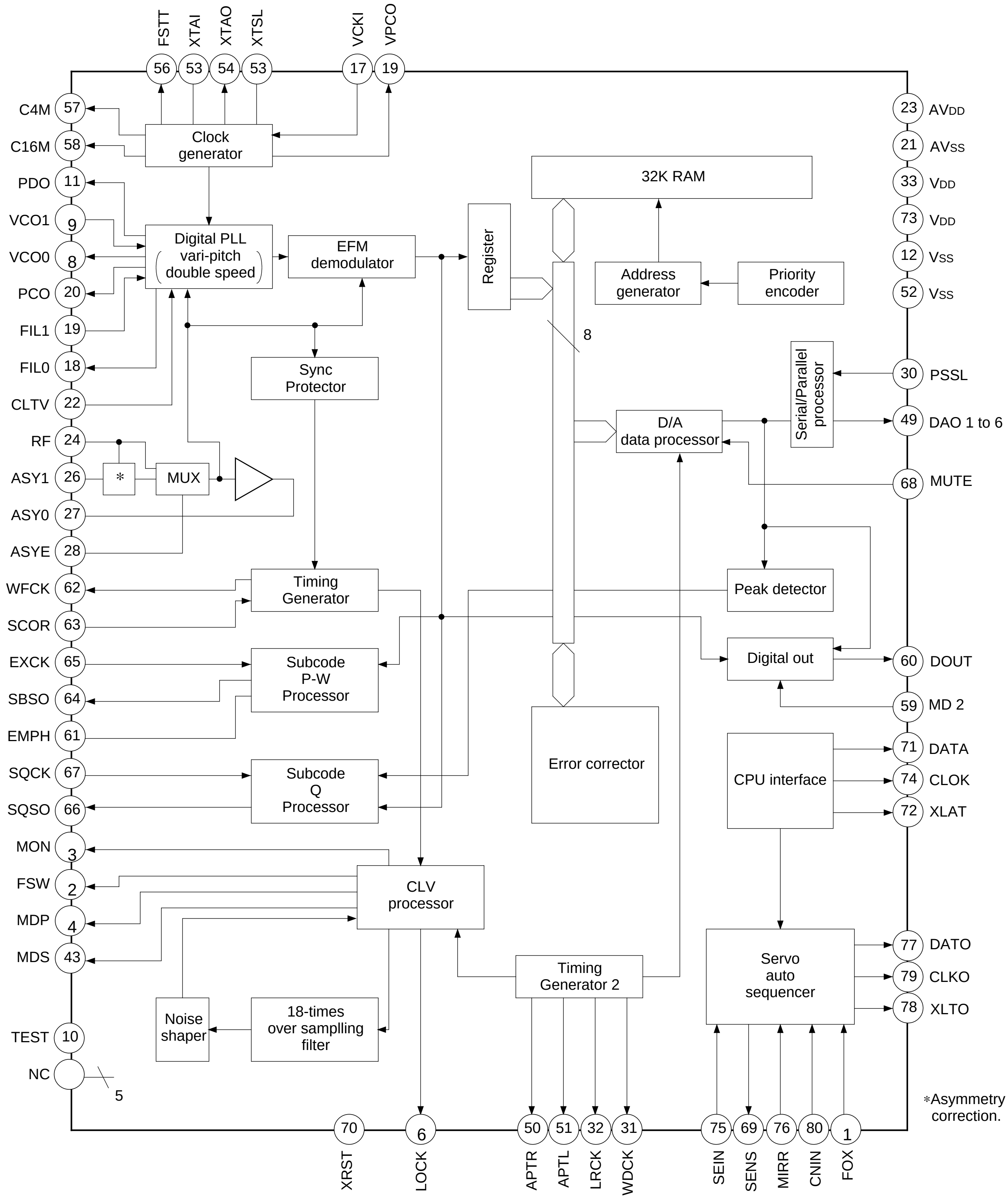
*3 V_{DD} value of 5.25 V (max.) is for the double-speed playback mode at vari-pitch control reset. For normal-speed playback and the low power consumption special playback mode, the V_{DD} value is 5.5 V (max.).

I/O Capacity

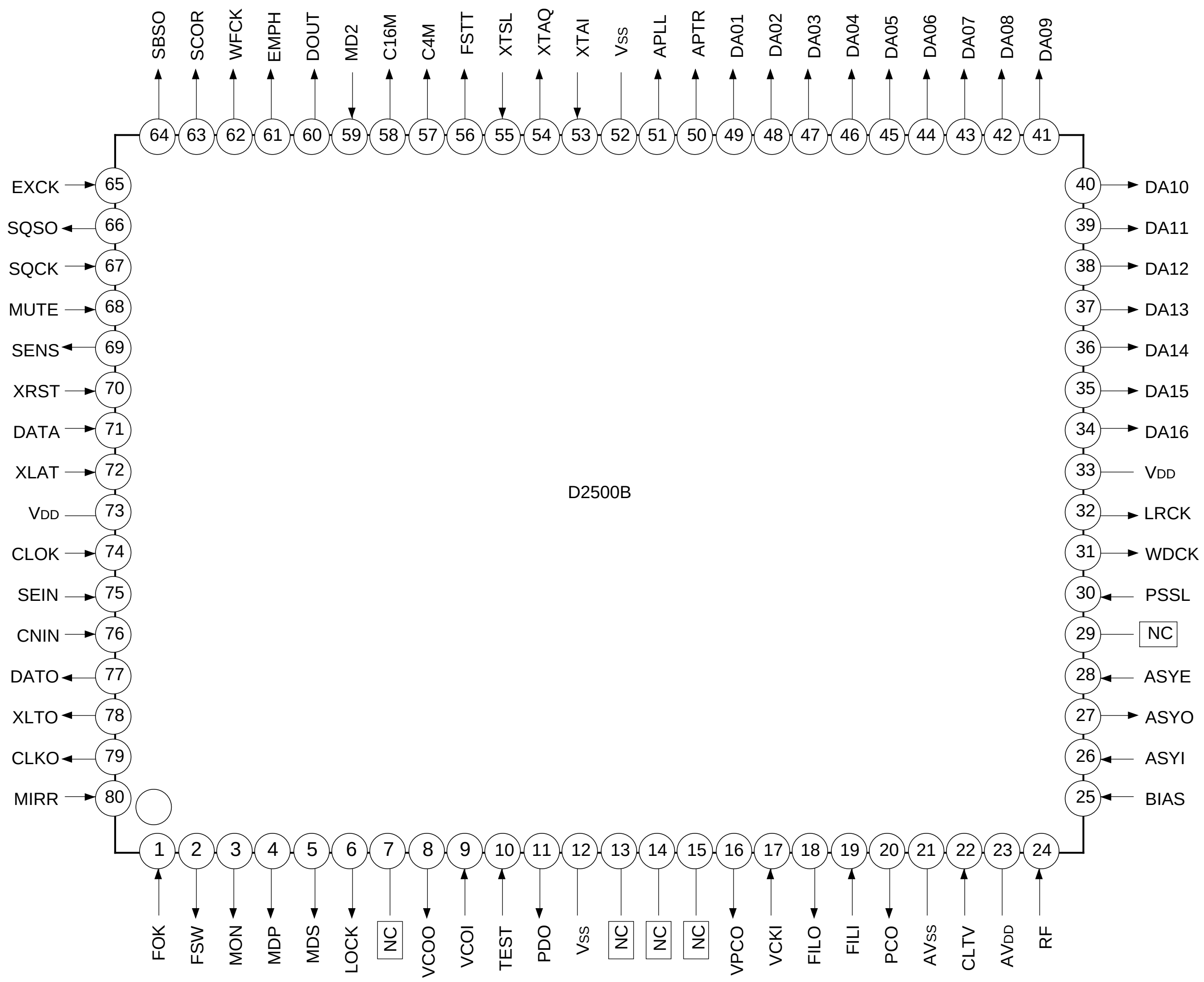
- Input pins CI 12 pF max.
- Output pins CO 12 pF max. at high impedance

Note: Test Conditions
V_{DD}=V_I=0 V
f_M=1 MHz

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O		Description
1	FOK	I		Focus OK input. Used for SENS output and servo auto sequencer.
2	FSW	O	Z, 0	Output used to switch the spindle motor output filter.
3	MON	O	1, 0	Output for spindle motor ON/OFF control
4	MDP	O	1, Z, 0	Output for spindle motor servo control
5	MDS	O	1, Z, 0	Output for spindle motor servo control
6	LOCK	O	1, 0	Output is “H” when the GFS signal sampled at 460 Hz is “H”. Output is “L” when the GFS signal is “L” 8 or more times in succession.
7	NC	—		
8	VCOO	O	1, 0	Output of oscillation circuit for analog EFM PLL
9	VCOI	I		Input to oscillation circuit for analog EFM PLL f_{LOCK}=8.6436 MHz
10	TEST	I		Test. Normally at 0 V (GND).
11	PDO	O	1, Z, 0	Output of charge pump for analog EFM PLL
12	V_{SS}			GND
13	NC	—		
14	NC	—		
15	NC	—		
16	VPCO	O	1, Z, 0	Output of charge pump for vari-pitch PLL
17	VCKI	I		Clock input from external VCO for vari-pitch control. fc_{center}=16.9344 MHz.
18	FILO	O	Analog	Output of filter for master PLL (Slave=Digital PLL)
19	FILI	I		Input to filter for master PLL
20	PCO	O	1, Z, 0	Output of charge pump for master PLL
21	AV_{SS}			Analog GND
22	CLTV	I		VCO control voltage input for master PLL
23	AV_{DD}			Analog power supply (+5 V)
24	RF	I		EFM signal input
25	BIAS	I		Asymmetry circuit constant current input
26	ASYI	I		Asymmetry comparator circuit voltage input
27	ASYO	O	1, 0	EFM full-swing output
28	ASYE	I		Asymmetry circuit OFF at “L”. Asymmetry circuit ON at “H”.
29	NC	—		
30	PSSL	I		Input used to switch the audio data output mode. “L” for serial output, “H” for parallel output.
31	WDCK	O	1, 0	D/A interface for 48-bit slot. Word clock f=2Fs
32	LRCK	O	1, 0	D/A interface for 48-bit slot. LR clock f=Fs
33	V_{DD}			Power supply (+5 V)
34	DA16	O	1, 0	Outputs DA16 (MSB) when PSSL=1, or serial data from the 48-bit slot (2’s complements, MSB first) when PSSL=0.
35	DA15	O	1, 0	Outputs DA15 when PSSL=1, or bit clock from the 48-bit slot when PSSL=0.
36	DA14	O	1, 0	Outputs DA14 when PSSL=1, or serial data from the 64-bit slot (2’s complements, LSB first) when PSSL=0.
37	DA13	O	1, 0	Outputs DA13 when PSSL=1, or bit clock from the 64-bit slot when PSSL=0.
38	DA12	O	1, 0	Outputs DA12 when PSSL=1, or LR clock from the 64-bit slot when PSSL=0.
39	DA11	O	1, 0	Outputs DA11 when PSSL=1, or GTOP when PSSL=0.
40	DA10	O	1, 0	Outputs DA10 when PSSL=1, or XUGF when PSSL=0.

Pin No.	Symbol	I/O		Description
41	DA09	O	1, 0	Outputs DA9 when PSSL=1, or XPLCK when PSSL=0.
42	DA08	O	1, 0	Outputs DA8 when PSSL=1, or GFS when PSSL=0.
43	DA07	O	1, 0	Outputs DA7 when PSSL=1, or RFCK when PSSL=0.
44	DA06	O	1, 0	Outputs DA6 when PSSL=1, or C2PO when PSSL=0.
45	DA05	O	1, 0	Outputs DA5 when PSSL=1, or XRAOF when PSSL=0.
46	DA04	O	1, 0	Outputs DA4 when PSSL=1, or MNT3 when PSSL=0.
47	DA03	O	1, 0	Outputs DA3 when PSSL=1, or MNT2 when PSSL=0.
48	DA02	O	1, 0	Outputs DA2 when PSSL=1, or MNT1 when PSSL=0.
49	DA01	O	1, 0	Outputs DA1 when PSSL=1, or MNT0 when PSSL=0.
50	APTR	O	1, 0	Control output for aperture correction. “H” for R-ch.
51	APTL	O	1, 0	Control output for aperture correction. “H” for L-ch.
52	VSS			GND
53	XTAI	I		Input for 16.9344 MHz and 33.8688 MHz X'tal oscillation circuit.
54	XTAO	O	1, 0	Output for 16.9344 MHz X'tal oscillation circuit.
55	XTSL	I		X'tal selection input. “L” for 16.9344 MHz X'tal, “H” for 33.8688 MHz X'tal.
56	FSTT	O	1, 0	2/3 frequency demultiplication output for Pins 53 and 54. Unaffected by vari-pitch control.
57	C4M	O	1, 0	4.2336 MHz output. Subject to vari-pitch control.
58	C16M	O	1, 0	16.9344 MHz output. Subject to vari-pitch control.
59	MD2	I		Digital-Out ON/OFF control. “H” for ON, “L” for OFF.
60	DOUT	O	1, 0	Digital-Out output.
61	EMPH	O	1, 0	“H” for playback disc provided with emphasis, “L” for without emphasis.
62	WFCK	O	1, 0	WFCK (Write Frame Clock) output.
63	SCOR	O	1, 0	“H” when subcode Sync S0 or S1 is detected.
64	SBSO	O	1, 0	Serial output of Sub P to W
65	EXCK	I		Clock input for reading SBSO
66	SQSO	O	1, 0	Outputs 80-bit Sub Q and 16-bit PCM peak-level data.
67	SQCK	I		Clock input for reading SQSO
68	MUTE	I		“H” for muting, “L” for release.
69	SENS	—	1, Z, 0	SENS output to CPU
70	XRST	I		System reset. “L” for resetting.
71	DATA	I		Inputs serial data from CPU.
72	XLAT	I		Latches serial data input from CPU at falling edge.
73	V_{DD}			Power supply (+5 V)
74	CLOCK	I		Inputs serial data transfer clock from CPU.
75	SEIN	I		Inputs SENSE from SSP.
76	CNIN	I		Inputs track jump count signal.
77	DATO	O	1, 0	Outputs serial data to SSP.
78	XLTO	O	1, 0	Latches serial data output to SSP at falling edge.
79	CLKO	O	1, 0	Outputs serial data transfer clock to SSP.
80	MIRR	I		Inputs mirror signal to be used by auto sequencer when jumping 16 or more tracks.

Note:

- The data at the 64-bit slot is output in 2's complements on an LSB-first basis. The data at the 48-bit slot is output in 2's complements on an MSB-first basis.
- GTOP monitors the state of Frame Sync protection. ("H": Sync protection window released)
- XUFG is a negative Frame Sync pulse obtained from the EFM signal before Frame Sync protection is effected..
- XPLCK is an inversion of the EFM PLL clock. The PLL is designed so that the falling edge of XPLCK coincides with a change point of the EFM signal.
- The GFS signal turns "H" upon coincidence between Frame Sync and the timing of interpolation protection.
- RFCK is a signal generated at 136-µs periods using a crystal oscillator.
- C2PO is a signal to indicate data error.
- XRAOF is a signal issued when a jitter margin of ±28F is exceeded by the 32K RAM.

Electrical Character

DC characteristics (V_{DD}=AV_{DD}=5.0 V±5 %, V_{SS}=AV_{SS}=0 V, Topr=–20 to +75°C)

Item			Condition	Min.	Typ.	Max.	Unit	Related pins
Input voltage (1)	Input voltage. “H” level	V_{IH} (1)		0.7V_{DD}			V	∗1
	Input voltage “L” level.	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	Input voltage “H” level	V_{IN} (2)	Schmitt circuit input	0.8V_{DD}			V	∗2
	Input voltage “L” level	V_{IN} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	V_{SS}		V_{DD}	V	∗3
Output voltage (1)	Output voltage “H” level	V_{OH} (1)	I_{OH}=–1 mA	V_{DD}–0.5		V_{DD}	V	∗4
	Output voltage “L” level	V_{OL} (1)	I_{OL}=1 mA	0		0.4	V	
Output voltage (2)	Output voltage “H” level	V_{OH} (2)	I_{OH}=–1 mA	V_{DD}–0.5		V_{DD}	V	∗5
	Output voltage “L” level	V_{OL} (2)	I_{OL}=2 mA	0		0.4	V	
Output voltage (3)	Output voltage “L” level	V_{OL} (3)	I_{OL}=2 mA	0		0.4	V	∗6
Output voltage (4)	Output voltage “H” level	V_{OH} (4)	I_{OH}=–0.28 mA	V_{DD}–0.5		V_{DD}	V	∗7
	Output voltage “L” level	V_{OL} (4)	I_{OL}=0.36 mA	0		0.4	V	
Input leak current		I_{LI}	V_I=0 to 5.25 V			±5	µA	∗1, ∗2, ∗3
Tristate pin output leak current		I_{LO}	V_O=0 to 5.25 V			±5	µA	∗8

Related pins

∗1 XTSL, DATA, XLAT, MD2, PSSL

∗2 CLOK, XRST, EXCK, SQCK, MUTE, FOK, SEIN, CNIN, MIRR, VCKI, ASYE

∗3 CLTV, FILI, RF

∗4 MDP, PDO, PCO, VPCO

∗5 ASYO, DOUT, FSTT, C4M, C16M, SBSO, SQSO, SCOR, EMPH, MON, LOCK, WDCK, DATO, CLKO, XLTO, SENS, MDS, DA01 to DA16, APTR, APTL, LRCK, WFCK

∗6 FSW

∗7 FILO

∗8 SENS, MDS, MDP, FSW, PDO, PCO, VPCO

AC Characteristics

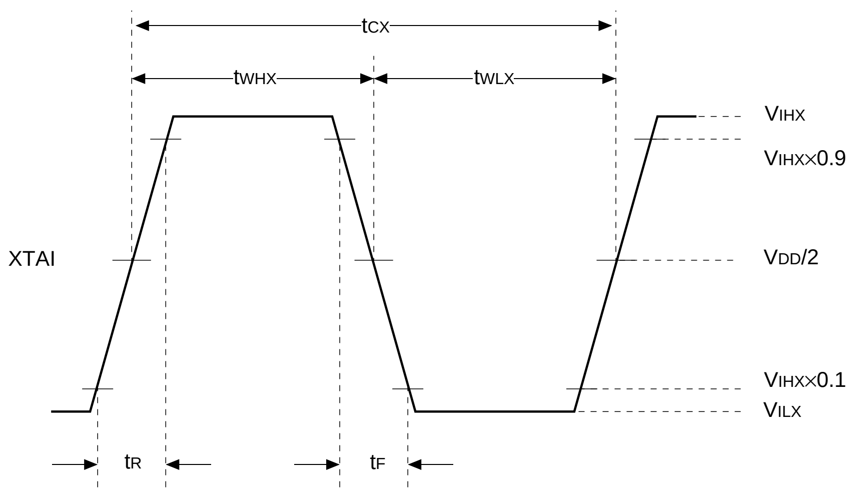
(1) XTAI and VCOI pins

1) During self-oscillation (Topr=–20 to +75 °C, $V_{DD}=AV_{DD}$=5.0 V±5 %)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

2) With pulses input to XTAI and VCOI pins (Topr=–20 to +75 °C, $V_{DD}=AV_{DD}$=5.0 V±5 %)

Item	Symbol	Min.	Typ.	Max.	Unit
"H" level pulse width	t_{WHX}	13		500	ns
"L" level pulse width	t_{WLX}	13		500	ns
Pulse period	t_{CX}	26		1,000	ns
Input "H" level	V_{IHX}	V_{DD}–1.0			V
Input "L" level	V_{ILX}			0.8	V
Rising time Falling time	t_R, t_F			10	ns



3) With sine waves input to XTAI and VCOI pins via capacitor

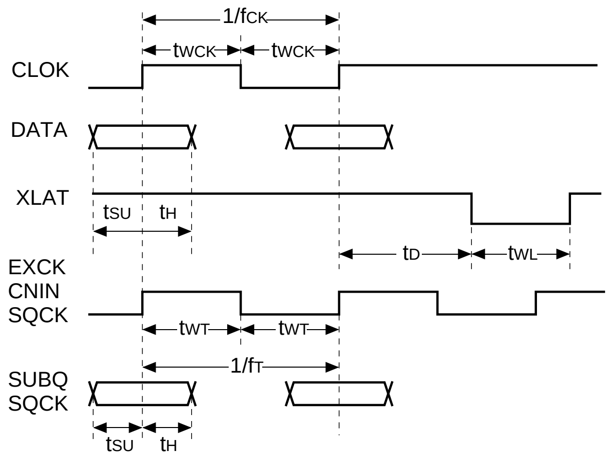
(Topr=–20 to +75 °C, $V_{DD}=AV_{DD}$=5.0 V±5 %)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_1	2.0		V_{DD}+0.3	Vp-p

(1) CLOK, DATA, XLAT, CNIN, SQCK, and EXCK pins

(V_{DD}=AV_{DD}=5.0 V±5 %, V_{SS}=AV_{SS}=0 V, Topr=–20 to +75 °C

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK, CNIN, SQCK frequency	f_T			1	MHz
EXCK, CNIN, SQCK pulse width	t_{WT}	300			ns



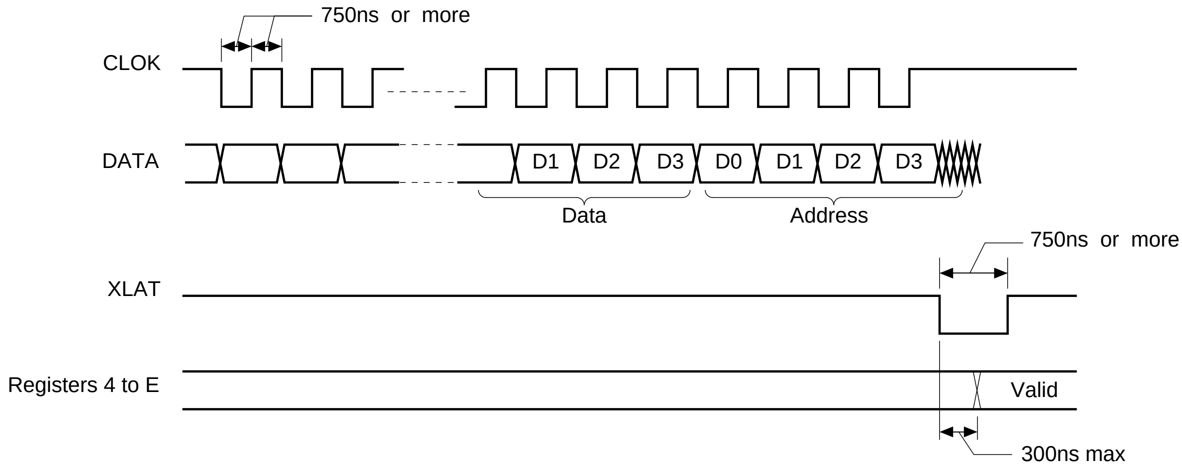
Description of Functions

§1 CPU Interface and Commands

• CPU interface

This interface is used to set various modes using DATA, CLOK, and XLAT.

The interface timing chart is shown below.



• The command addresses of the CXD2500B and the data capable of being set are shown in Table 1-1.

• When XRST is set to 0, the CXD2500B is reset, causing its internal registers to be initialized to the values listed in Table 1-2.

Commands

Register name	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C)	0	1	0	1	0.18 ms	0.09 ms	0.045 ms	0.022 ms	—	—	—	—	—	—	—	—	—	—	—	—
	Brake (B)					0.36 ms	0.18 ms	0.09 ms	0.045 ms												
6	KICK (D)	0	1	1	0	11.6 ms	5.8 ms	2.9 ms	1.45 ms	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequencer track jump (N) setting	0	1	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CDROM	0	D OUT Mute-F	WSEL	—	—	—	—	—	—	—	—	—	—	—	—
9	Func specification	1	0	0	1	D CLV ON-OFF	DSPB ON-OFF	A SEQ ON-OFF	D PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	Vari UP	Vari Down	Mute	ATT	PCT1	PCT2	—	—	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	32,768	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1
C	Servo factor setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CRTL	1	1	0	1	DCLV PWM MD	TB	TP	CLVS Gain	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	CM3	CM2	CM1	CM0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-1

Reset Initialization

Register name	Command	Address				Data 1				Data 2				Data 3				Data 3			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
5	Blind (A, E), Overflow (C) Brake (B)	0	1	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—
6	KICK (D)	0	1	1	0	0	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—
7	Auto sequencer track jump setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
9	Func specification	1	0	0	1	1	0	0	1	0	0	0	—	—	—	—	—	—	—	—	—
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	—	—	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Servo factor setting	1	1	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—	—	—
D	CLV CRTL	1	1	0	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
E	CLV mode	1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1-2

§1 Meanings of Data Set at Command Addresses

$4X Command

Command	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS-ON	0	1	1	1
1 TRACK JUMP	1	0	0	RXF
10 TRACK JUMP	1	0	1	RXF
2N TRACK JUMP	1	1	0	RXF
M TRACK MOVE	1	1	1	RXF

RXF=0 FORWARD
RXF=1 REVERSE

- If a Focus-ON command ($47) is canceled during execution, $02 is issued and the auto sequence operation is discontinued.
- If a Track Jump or Track Move command ($48 to $4F) is canceled during execution, the auto sequence operation is discontinued.

$5X Command

Used to set timers for the auto sequencer.

Timers set: A, E, C, and B

Command	D3	D2	D1	D0
Blind(A, E), Overflow(C)	0.18 ms	0.09 ms	0.045 ms	0.022 ms
Brake(B)	0.36 ms	0.18 ms	0.09 ms	0.045 ms

Example: D2=D0=1, D3=D1=0 (Initial Reset)
A=E=C=0.112 ms
B=0.225 ms

$6X Command

Used to set a timer for the auto sequencer.

Timer set: D

Command	D3	D2	D1	D0
KICK (D)	11.6 ms	5.8 ms	2.9 ms	1.45 ms

Example: D3=0 D2=D1=D0=1 (Initial Reset)
D=10.15ms

$7X Command

Used to set the number of auto sequencer track jumps/moves.

Command	Data3				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequencer track jump number setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command sets the value of “N” for 2N track jump and M track move execution using the auto sequencer.

- The maximum number of tracks that can be counted is 65,535. However, in the case of 2N track jumps, it is subject to mechanical restrictions due to the optical system.
- When the number of tracks to be jumped is smaller that 15, the signals input from CNIN are counted. When it is 16 or larger, the signals input from the MIRR pin are counted. This count signal selection contributes toward improving the accuracy of high-speed track jumping.

Command	D3	D2	D1	AS0
MODE specification	CDROM	0	D. OUT Mute-F	WSEL

$8X Command

Command	C2PO timing	Processing
CDROM=1	1-3	CDROM mode is entered. In this mode, average value interpolation and preceding value holding are not performed.
CDROM=0	1-3	Audio mode is entered. In this mode, average value interpolation and preceding value holding are performed.

Command bit	Processing
D. out Mute F=1	When Digital Out is ON (pin MD2=1), DA output is muted.
D. out Mute F=0	Da output muting is unaffected by the setting of Digital Out.

D/A Out D.out Mute with F=1

	MD2=1 (D. out-ON)	MD2=0 (D. out-OFF)
Mute-ON	– ∞dB	– ∞dB
Mute-OFF	– ∞dB	0dB

Command bit	Sync protection window width	Application
WSEL=1	±26 channel clock pulses*	Anti-rolling is enhanced.
WSEL=0	±6 channel clock pulses	Sync window protection is enhanced.

* In normal-speed playback, the channel clock frequency is 4.3218 MHz.

$9X Command

Command	Data 1				Data 2		
	D3	D2	D1	D0	D3	D2	D1
Func specification	DCLV ON-OFF	DSPB ON-OFF	A. SEQ ON-OFF	D. PLL ON-OFF	BiliGL MAIN	BiliGL Sub	FLFC

<table>
<tr><th>Command bit</th><th>CLV mode</th><th colspan="2">Contents</th></tr>
<tr><td rowspan="2">DCLV ON-OFF=0</td><td>In CLVS mode</td><td colspan="2">FSW=L, MON-H, MDS-Z, MDP=servo control signal, with carrier frequency of 230 Hz at T_B=0 and 460 Hz at T_B=1</td></tr>
<tr><td>In CLVP mode</td><td colspan="2">FSW=Z, MON=H, MDS=speed control signal with carrier frequency of 7.35 kHz, MDP=phase control signal with carrier frequency of 1.84 kHz</td></tr>
<tr><td rowspan="2">DCLV ON-OFF=1
(FSW and MON are unnecessary)</td><td rowspan="2">In CLVS or CLVP mode</td><td>DCLV when PWM, MD=1</td><td>MDS= PWM polarity signal. Carrier frequency=132 kHz
MDS= PWM absolute value output (binary). Carrier frequency=132 kHz</td></tr>
<tr><td>DCLV when PWM, MD=0</td><td>MDS= Z
MDP= ternay PWM output.
Carrier frequency=132 kHz</td></tr>
</table>

In the Digital CLV servo mode with DCLV ON-OFF set to 1, the sampling frequency of the internal digital filter is switched at the same time as the switching between CLVP and CLVS.
Therefore, for CLVS, the cut-off frequency fC is 70 Hz when T_B is set to 0, and 140Hz when T_B is set to 1.

Command bit	Processing
DSPB=0	Normal-speed playback. ECC quadruple error correction is made. Vari-pitch control is enabled.
DSPB=1	Double-speed playback. ECC double error correction is made. Vari-pitch control is disabled.

Set FLFC at 1 when in double-speed playback mode (exclude the low power consumption special playback mode). However, FLFC can be set to 0 during PLL pull-in (lock). Set to 0 for all other modes.

SENS Output

Microcomputer serial register values (Latching unnecessary)	ASEQ=0	ASEQ=1
$0X	Z	SEIN (FZC)
$1X	Z	SEIN (A, S)
$2X	Z	SEIN (T. Z. C)
$3X	Z	SEIN (SSTOP)
$4X	Z	XBUSY
$5X	Z	FOK
$6X	Z	SEIN (Z)
$AX	GFS	GFS
$BX	COMP	COMP
$CX	COUT	COUT
$EX	$\overline{OV64}$	$\overline{OV64}$
$7X, 8X, 9X, DX, FX	Z	0

Description of SENS signals

SENS output	Meaning
Z	SENS is at High-Z state.
SEIN	SEIN signal, which was input to the CXD2500B, is output from SSP.
XBUSY	“L” when auto sequencer is in operation; “H” when terminated.
FOK	Output of the signal (normally FOK input from RF) input to the FOK pin. “H” when Focus OK is received.
GFS	“H” when regenerated Frame Sync is obtained at the correct time.
COMP	Used in counting the number of tracks set in register B. “H” when the count is latched to register B twice in succession. It is reset to “L” level when the count of CNIN inputs equals the originally set number for register B.
COUT	Used in counting the number of tracks set in register B. “H” when the count is latched to register B, then to register C. It is toggled every time the count of CNIN inputs reaches the value set in register B.
OV64	“L” when after passing through the sync detection filter, the EFM signal become longer than the 64 channel clocks.

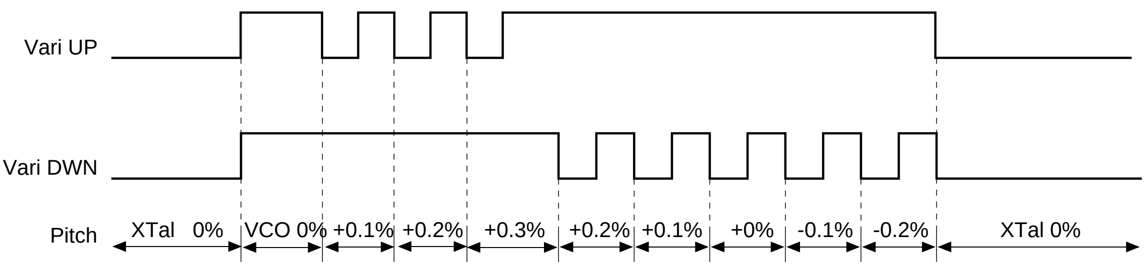
Command bit	Meaning
DPLL=0	RFPLL enters analog mode. PDO, VCOI, and VCOO are used.
DPLL=1	RFPLL enters digital mode. PDO becomes Z.

Command bit	BiliGL MAIN=0	BiliGL MAIN=1
BiliGL SUB=0	STEREO	MAIN
BiliGL SUB=1	SUB	Mute

Definition of Bilingual MAIN, SUB, and STEREO
MAIN; The input L-ch signal is output to both L-ch and R-ch.
Sub: The input R-ch signal is output to both L-ch and R-ch.
STEREO: The input L-ch and R-ch signals are output to both L-ch and R-ch respectively.

$AX Command

Command	Data 1				Data 2	
	D3	D2	D1	D0	D3	D2
Audio CTRL	Vari UP	Vari DWN	Mute	ATT	PCT1	PCT2



Command bit	Meaning
Mute=0	Muting is off unless condition to make muting occurs.
Mute=1	Muting is on. Peak register reset.

Command bit	Meaning
ATT=0	Attenuation is off.
ATT=1	–12dB

Condition for Muting

(1) Mute=1 in register A
(2) Pin Mute=1
(3) D.OUT Mute F=1 in register 8 with D.Out ON (MD2=1)
(4) Elapse of over 35 msec after GFS turns "Low"
(5) BiliGL MAIN=Sub=1 in register 9
(6) PCT1=1 and PCT2=2 in register A

In the case of (1) to (4), zero-cross muting not exceeding 1 msec is performed.

Command bit		Meaning	PCM Gain	ECC correction capacity
PCT1	PCT2			
0	0	Normal mode	×0 dB	C1: Double, C2: Quadruple
0	1	Level meter mode	×0 dB	C1: Double, C2: Quadruple
1	0	Peak meter mode	Mute	C1: Double, C2: Double
1	1	Normal mode	×0 dB	C1: Double, C2: Double

Level Meter Mode (See Timing Chart 1-4.)

- This mode makes the digital level meter function available.
- Inputting 96-bit clock pulses to SQCK will enable 96 data to be output to SQSO. Of the output data, the first 80 bits comprise Sub-Q data, which transmit the description for the data format to the Sub Code interface.
  The last 16 bits are ordered LSB-first, of which the first 15 bits constitute PCM data (absolute value). The final 1 bit is "High" if the prior PCM data was generated at the left channel; "Low" if generated at the right channel.
- The PCM data is reset once it is read, and the L/R flag is reversed. While this state is kept until the next read operation is started, testing for the maximum value is conducted.

Peak Meter Mode (See Timing Chart 1-5.)

- In this mode, the maximum value of PCM data is detected whether the channel involved is L-ch or R-ch. To read the detected maximum value, it is necessary to input 96 clock pulses to SQCK.
- When 96 clock pulses have been input to SQCK, 96 bits of data is output to SQSO. At the same time, the data is re-set in an internal register of the LSI.
  That is, the PCM peak detection register is not reset when it is read.
- To reset the PCM peak register, set both PCT1 and PCT2 to 0. Or, Set $AX mute.
- In this mode, the absolute time of Subcode Q is controlled automatical.
- Namely, every time a peak value is detected, the absolute time when the CRC was passed is stored. The program time operation is performed in the normal way.
- The last bit (L/R flag) of the 96-bit data stays 0.
- In this mode, the preceding value holding and average value interpolation data are fixed to level (–∞).

$CS Command

Command	D3	D2	D1	D0	Explanation
Servo factor setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Only DCLV=1 is effective.
CLV CTRL ($DX)				Gain CLVS	DCLV=1 and DCLV=0 are both effective.

This command is used to externally set the spindle servo gain when DCLV=1.

• Gain setting for CLVS mode: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note: When DCLV=0, the CLVS gain is determined as follows:
If Gain CLVS=0, then GCLVS=–12 dB.
If Gain CLVS=1, then GCLVS=0 dB

• Gain setting for CLVP mode: GMDP, GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6 dB
0	1	0 dB
1	0	+ 6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

$DC Command

Command	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	CLVS Gain

See "$CX Command."

Command bit	Description (See Timing Chart 1-6.)
DCLV PWM MD=1	Specification of PWM mode for digital CLV. Both MDS and MDP are used.
DCLV PWM MD=0	Specification of PWM mode for digital CLV. Ternary MDP values are output.

Command bit	Description
TB=0	In CLVS or CLVH mode, bottom value is held at periods of RFCK/32.
TB=1	In CLVS or CLVH mode, bottom value is held at periods of RFCK/16.
TP=0	In CLVS mode, peak value is held at periods of RFCK/4.
TP=1	In CLVS mode, peak value is held at periods of RFCK/2.

In CLVH mode, peak holding is made at 34 kHz.

$EX Command

Command	D3	D2	D1	D0
CLV mode	CM3	CM2	CM1	CM0

CM3	CM2	CM1	CM0	Mode	Explanation
0	0	0	0	STOP	See Timing Chart 1-7.
1	0	0	0	KICK	See Timing Chart 1-8.
1	0	1	0	BRAKE	See Timing Chart 1-9.
1	1	1	0	CLVS	
1	1	0	0	CLVH	
1	1	1	1	CLVP	
0	1	1	0	CLVA	

STOP: Spindle motor stop mode

KICK: Spindle motor forward run mode

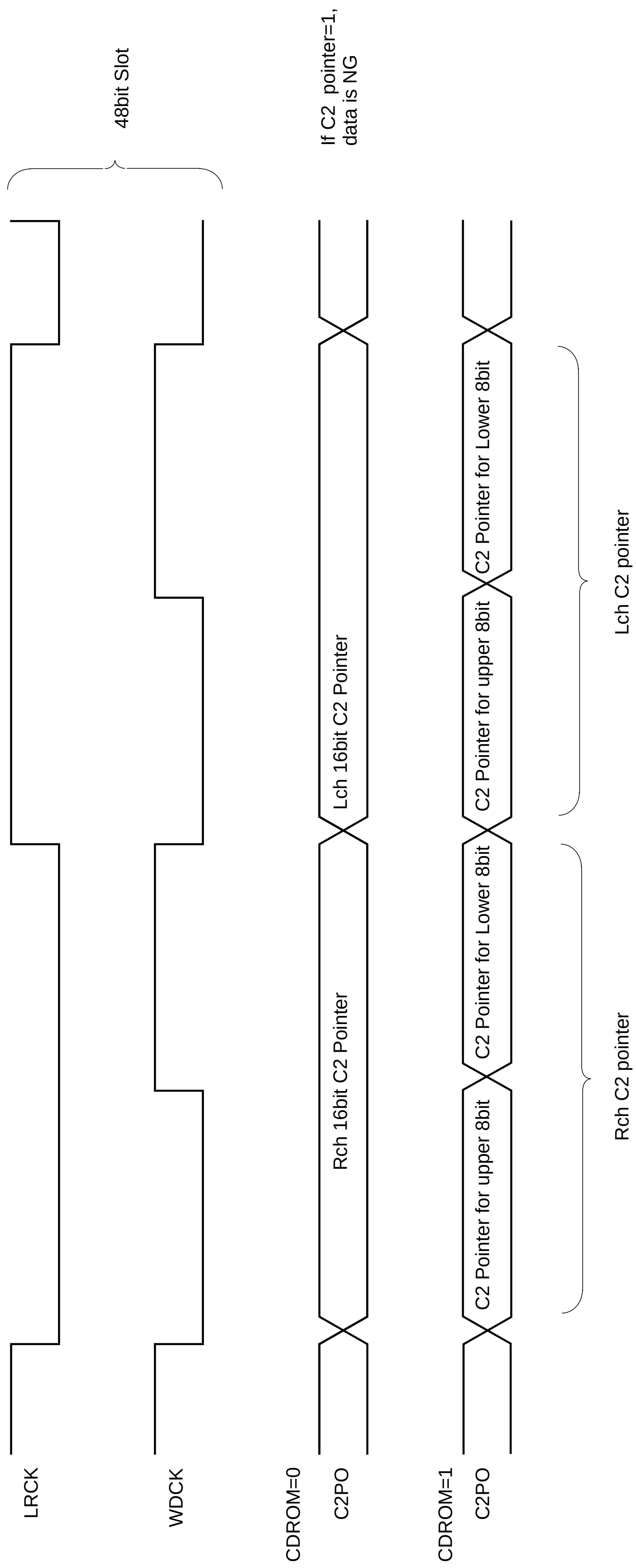
BRAKE: Spindle motor reverse run mode

CLVS: Rough servo mode for use for pulling disc run into RF-PLL capture range when the RF-PLL circuit lock has been disengaged

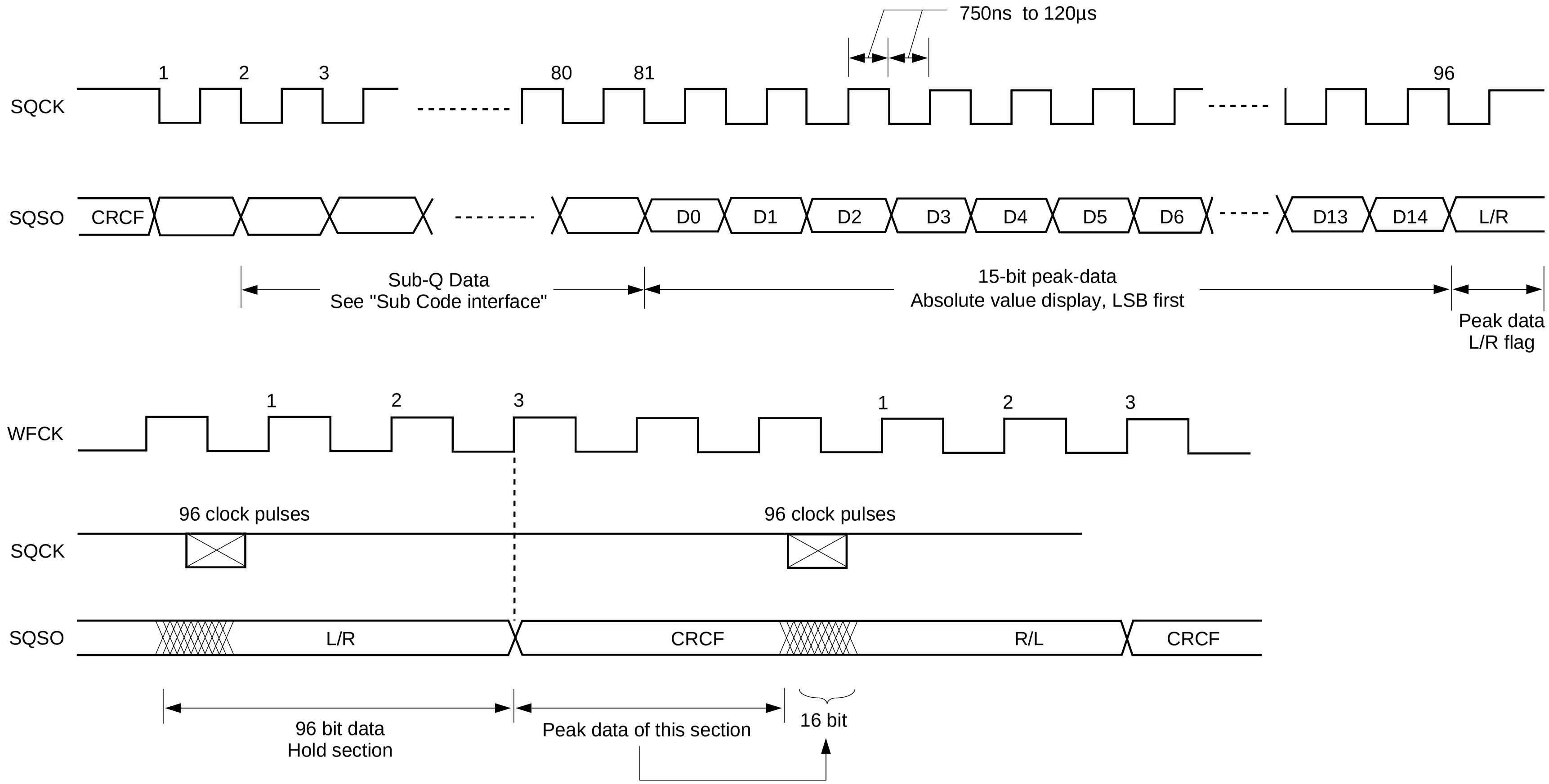
CLVP: PLL servo mode

CLVA: Automatic switching mode for CLVS and CLVS. This mode is used during normal play status.

Timing Chart 1-3

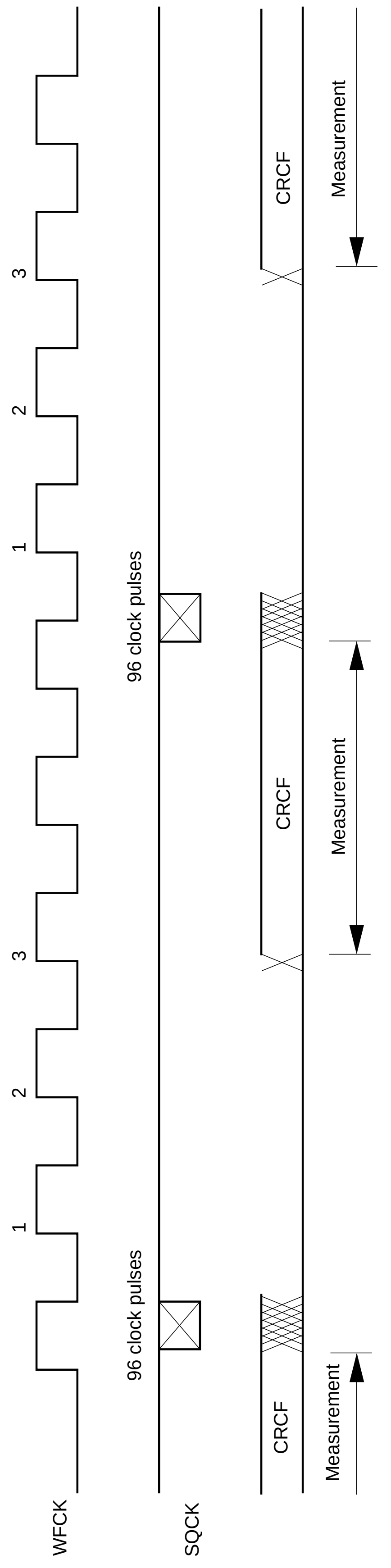


Timing Chart 1-4



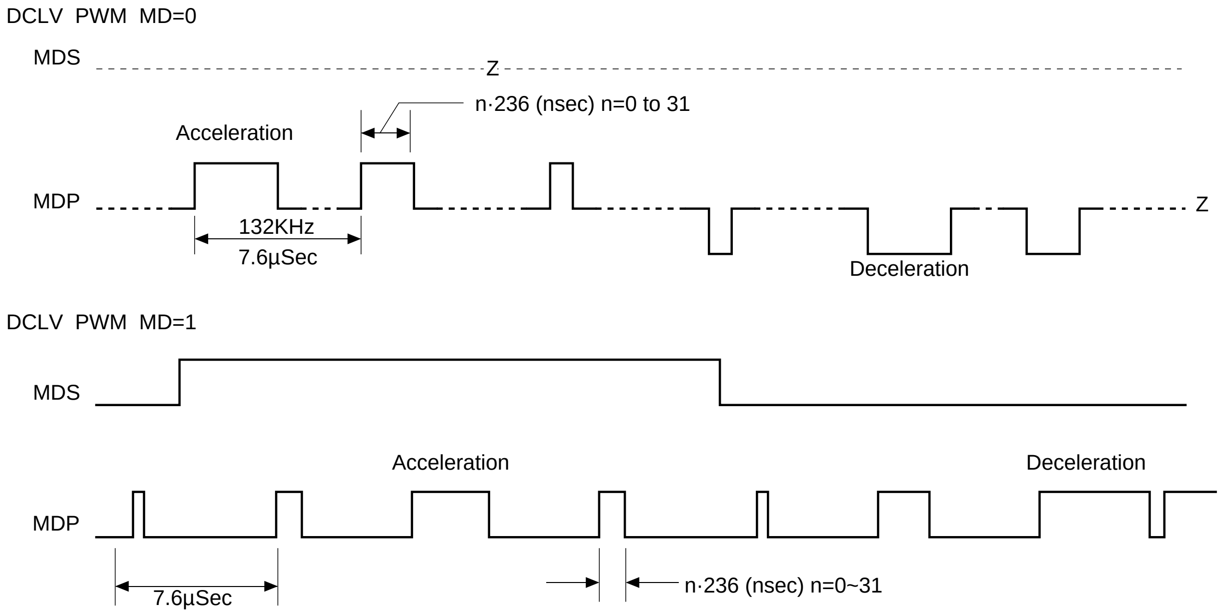
Level Meter Timing

Timing Chart 1-5



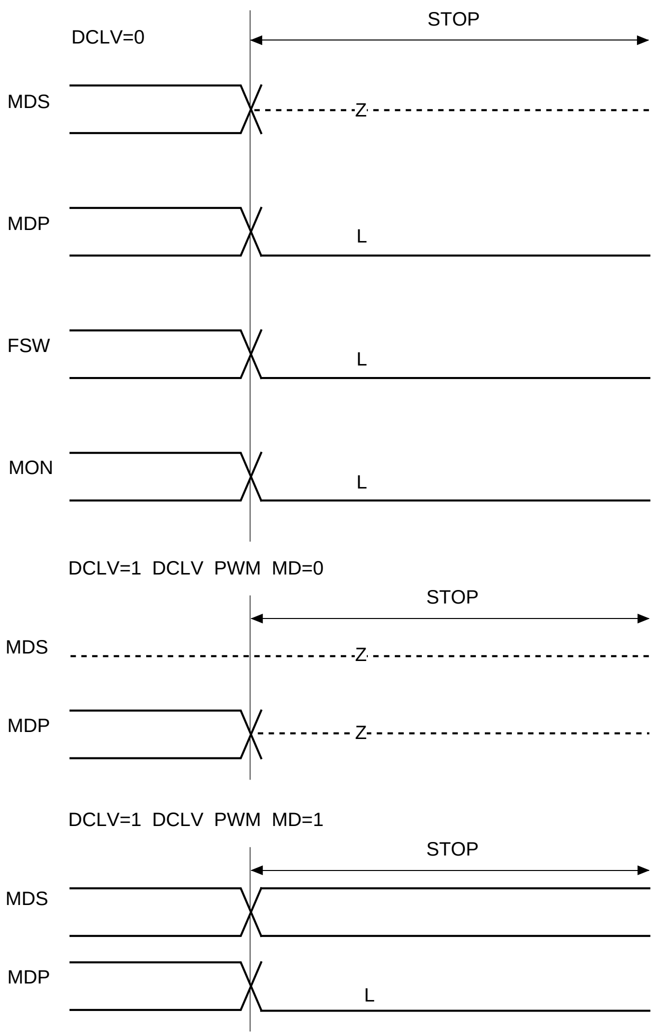
Peak Meter Timing

Timing Chart 1-6



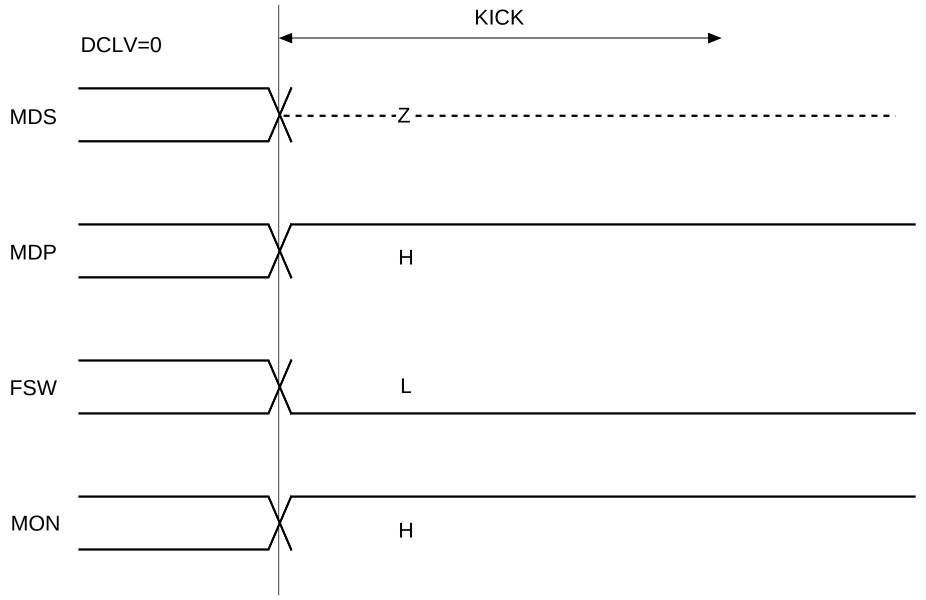
Output Waveforms with DCLV=1

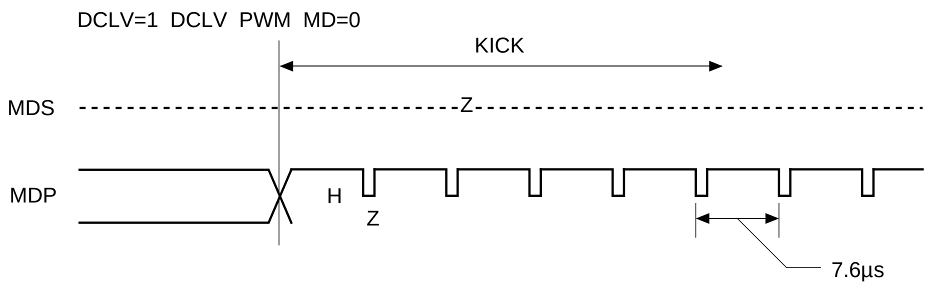
Timing Chart 1-7



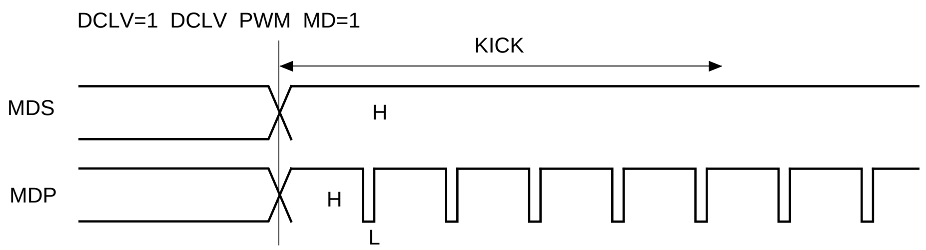
FSW and MON are the same as for DCLV=0

Timing Chart 1-8



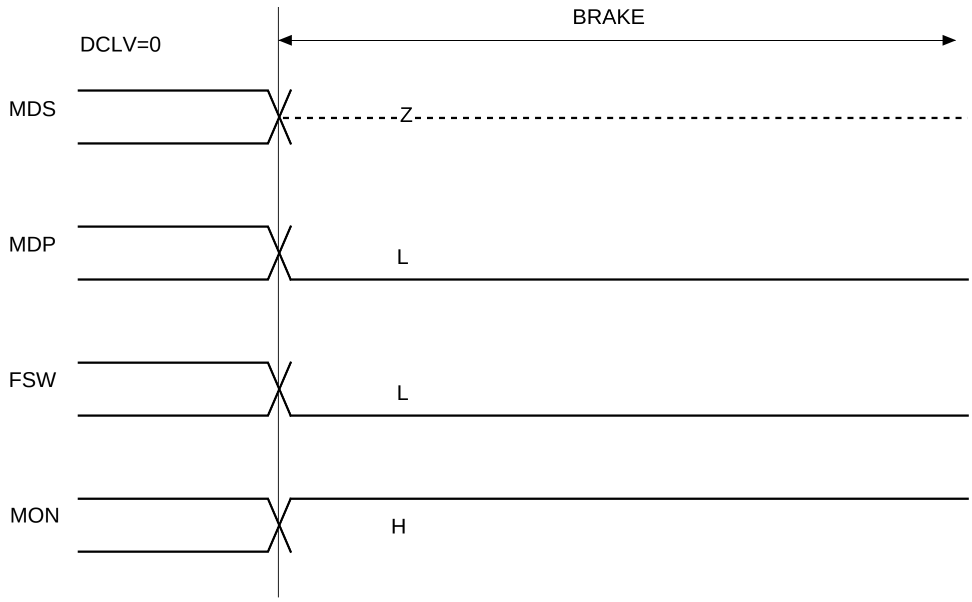


FSW and MON are the same as for DCLV=0

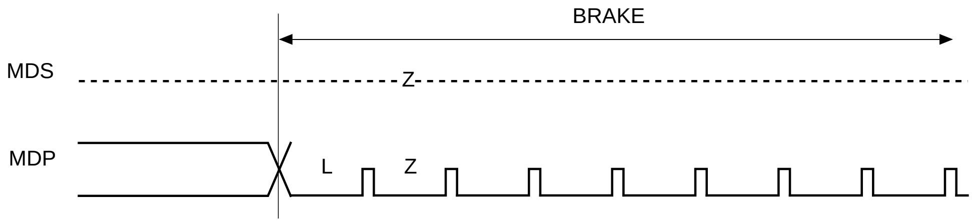


FSW and MON are the same as for DCLV=0

Timing Chart 1-9

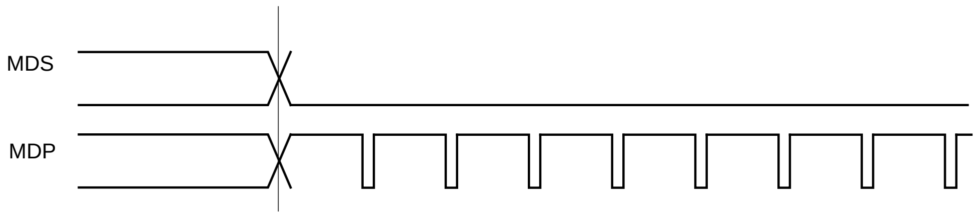


DCLV=1 DCLV PWM MD=0



FSW and MON are the same as for DCLV=0

DCLV=1 DCLV PWM MD=1



FSW and MON are the same as for DCLV=0

§2 Subcode Interface

In this section, the subcode interface will be explained.
The contents of the subcode interface can be externally read in two ways. The subcodes P through W totaling 8 bits can be read from SBSO by inputting EXCK to the CXD2500B.
Sub-Q can be read after conducting a CRC check on the 80bits of information in the subcode frame. First, check SCOR and CRCF, then input 80 clock pulses to SQCK and read the data.

§2-1 P-W Subcode Read

These subcodes can be read by entering EXCK immediately after the fall of WFCK. (See Timing Chart 2-1.)

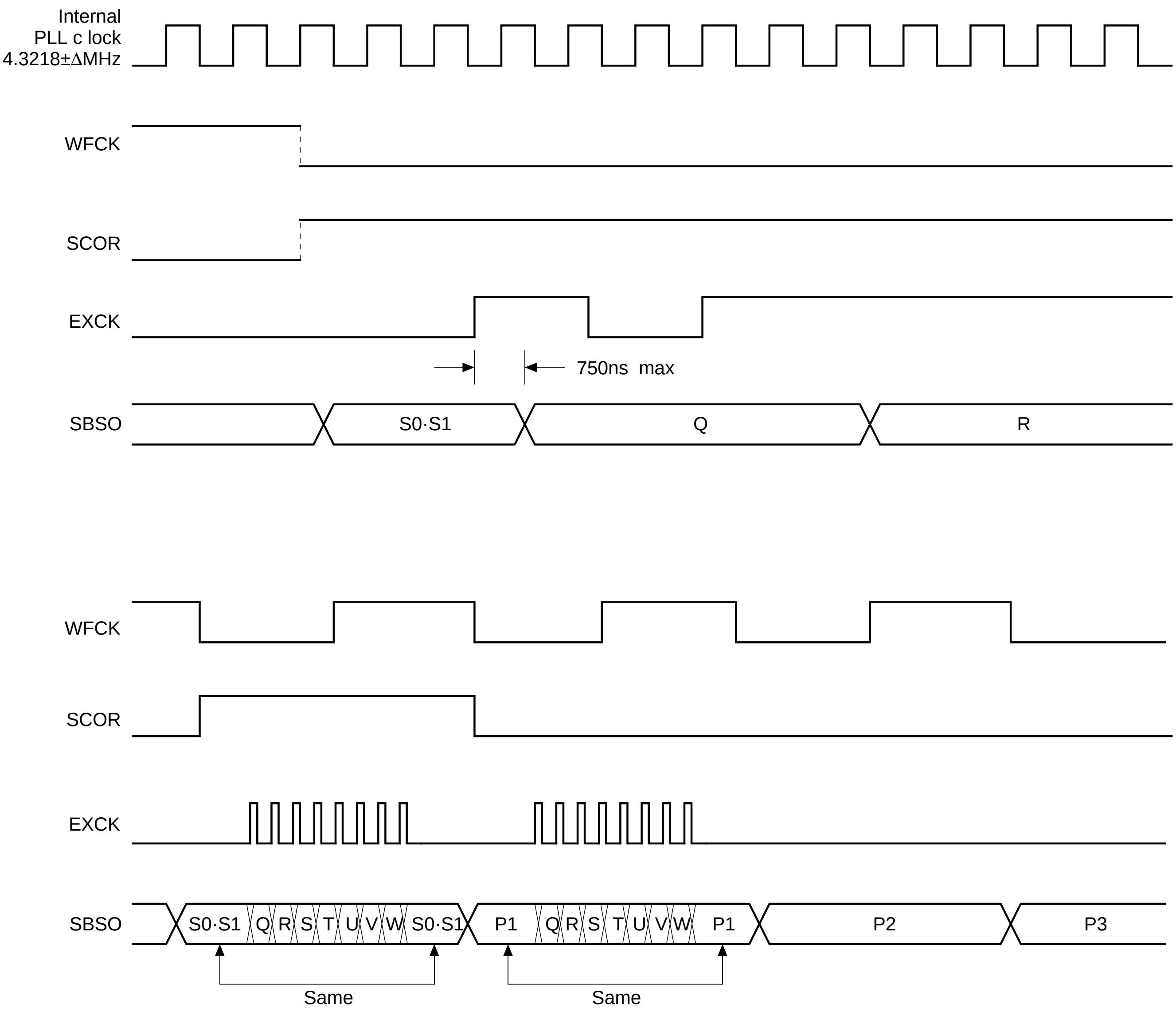
§2-2 80-bit Sub-Q Read

Figure 2-2 shows a block diagram of the peripheral part of the 80-bit Sub-Q register.

- The Sub Q regenerated on a bit-per-frame basis is input to the 80-bit serial/parallel register and the CRC circuit.
- When the results of CRC of the 96-bit Sub-Q are OK, CRCF is set to 1 and the 96-bit data is output to SQSO.
  Furthermore, it is loaded into the 80-bit, parallel/serial register.
  If SQSO is “H” after the output of SCOR, it can be taken that CPU has been loaded a new set of CRCOK data.
- When 80-bit data is loaded into CXD2500B, MSB and LSB are reversed within each byte of the data.
  Therefore, the bits are ordered LSB-first within each byte, even though the byte arrangement is kept unchanged.
- When 80 bits of data are confirmed to have been loaded, SQCK is input to read the data. Subsequently in the CXD2500B, the input of SQCK is detected and the retriggerable monostable multivibrator is reset during Low.
- The time constant of the retriggerable monostable multivibrator ranges from 270 to 400 µs. If the time of High for SQCK is less than this time constant, the monostable multivibrator will keep resetting, preventing the contents of the P/S register from being loaded into the P/S register.
- While the monostable multivibrator is resetting, data loading into the peak detection parallel/serial register and 80-bit parallel/serial register is forbidden.
  Therefore, while data read operation is carried out at clock periods shorter than the time constant of the monostable multivibrator, the contents of these registers are retained without being rewritten by CRCOK, etc.
- The CXD2500B permits the peak detection register to be connected to the shift-in of the 80-bit P/S register.
  For Ring Control 1, the input and output are short-circuited during peak meter and level meter mode.
  For Ring Control 2, the input and output are short-circuited during peak meter mode only.
  The Ring Controls are arranged in this way in order for the registers to be reset each time their contents are read in the level meter mode, while preventing destructive read in the peak meter mode.
  To enable this control, 96 clock pulses must be input to the peak meter mode.
- As afore mentioned, in the peak meter mode, the absolute time following the generation of a peak value is stored.
  These operations are shown in Time chart 2-3.

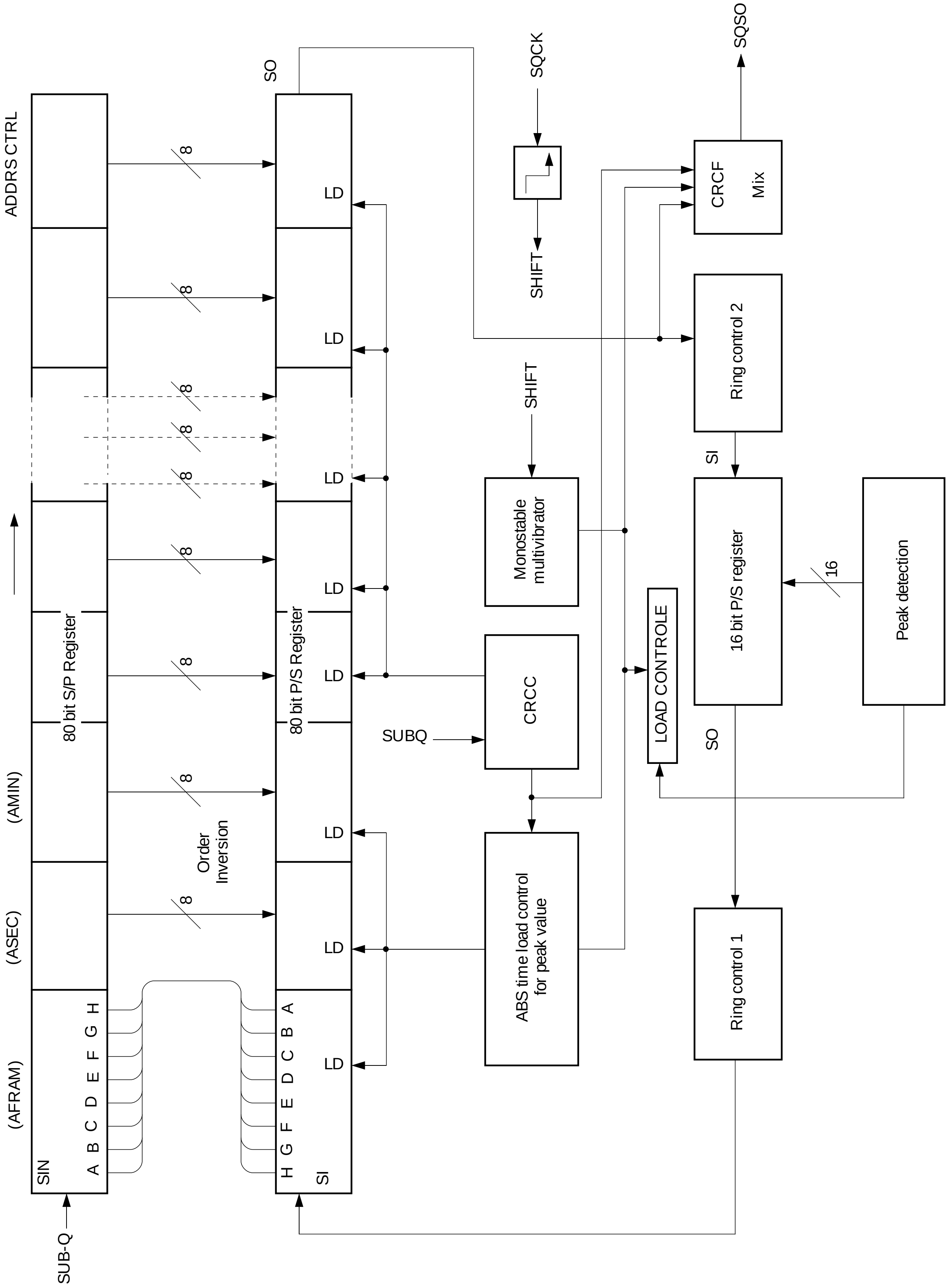
Note: To perform the above operations, the duration of the clock pulse input to SQCK must be between 750ns and 120 µs for both “High” and “Low”.

Timing Chart 2-1

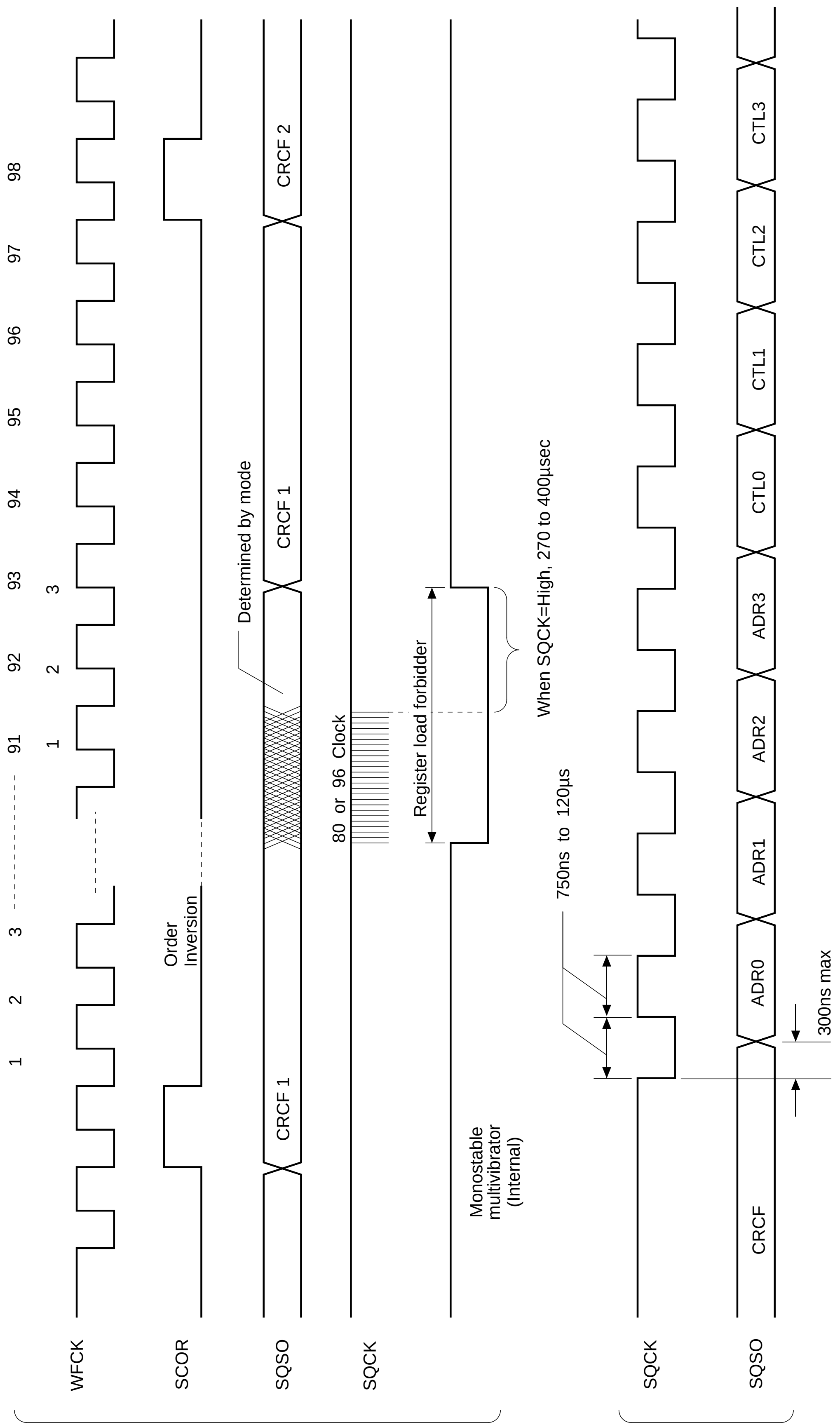


Subcode P. Q. R. S. T. U. V. W Read Timing

Block Diagram 2-2



Timing Chart 2-3

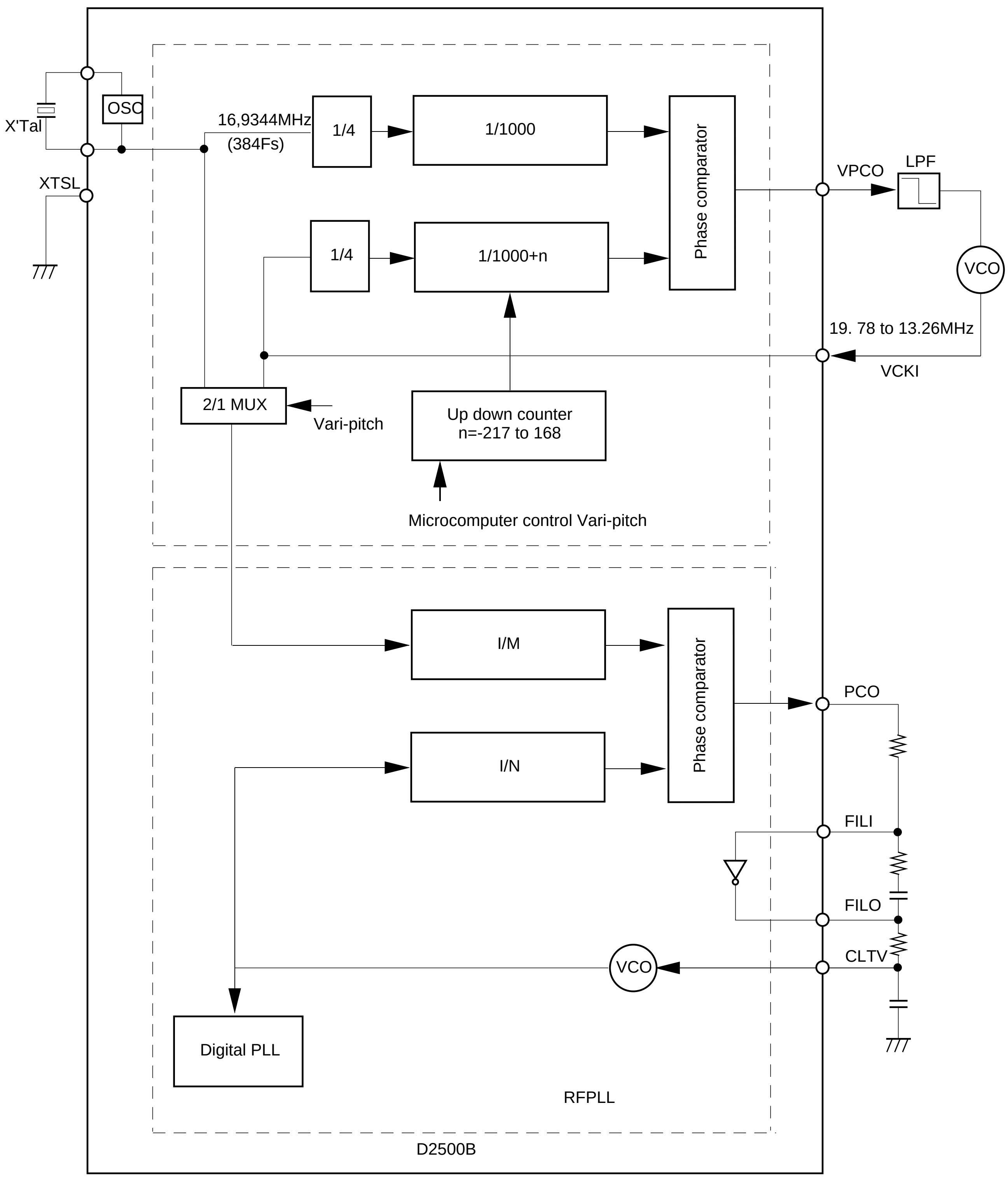


§3 Other Functions

§3-1 Channel Clock Regeneration Using Digital PLL Circuit

- Demodulation of regenerated EFM signals using an optical system requires the use of channel clock pulses.
  The EFM signal to be demodulated has been modulated into an integer multiple of the channel clock period T, ranging from 3T to 11T.
  To read the information conveyed by the EFM signal, it is essential to correctly recognize the integral value; hence, the need to use channel clock pulses.
  In an actual CD player, the pulse width of the EFM signal will vary, affected by fluctuations of the disc rotation. For this reason, it is necessary to use a PLL in regenerating channel clock pulses.
  Figure 3-1 shows a block diagram of the 3-stage PLL contained in the CXD2500B.
- The 1st-stage PLL is used for vari-pitch regeneration. To use this PLL, LPF and VCO are necessary as external parts.
  The minimum pitch variable possible is 0.1 %. The output of this 1st-stage PLL is used as the standard for all the clock pulses used in the LSI.
  When vari-pitch control is not in uses, connect the output pin of XTAO to VCKI.
- The 2nd-stage PLL generates high frequency clock pulses necessary for the 3rd-stage digital PLL.
- The 3rd-stage comprises a digital PLL used to regenerate the actual channel clock pulses. It realizes a capture range of ±150 kHz (normal conditions) or more.
- The digital PLL features a secondary loop. It is controlled through the primary loop (phase) secondary loop (frequency).
  When FLFC=1, the secondary loop can be turned off.
- When high frequency components such as 3T, 4T, are deviated, turning off the secondary loop will provide better play ability.
- However, the capture range will be 50 kHz.

Block Diagram 3-1



§3-2 Frame Sync Protection

- During CD player operation at normal speed, Frame Sync is recorded approximately once every 136 µs (at 7.35 kHz).
  This signal can be used to identify the data within each frame. When Frame Sync cannot be recognized, the data also cannot be identified; as a result, it is treated as an error. Therefore, correct Frame Sync recognition is very important to ensure high play ability for the CD player.
- The CXD2500B employs window protection, front protection and rear protection to realize a powerful Frame Sync protection. The CXD2500B offers two window widths, one for use when the player is subjected to rotational disturbance and the other for use without such disturbance (WSEL=0/1).
  The front protection counter is fixed at 13 and the rear protection counter at 3. Therefore, during normal play back, when the frame sync cannot be detected due to damages on the disc. If the number to frames with undetected Frame Sync exceeds 13, the window is released and the Frame Sync signal are re-synchronized. If no Frame Sync is correctly detected in 3 successive frames immediately after Frame Sync re-synchronization performed following a window release, the window is released at once.

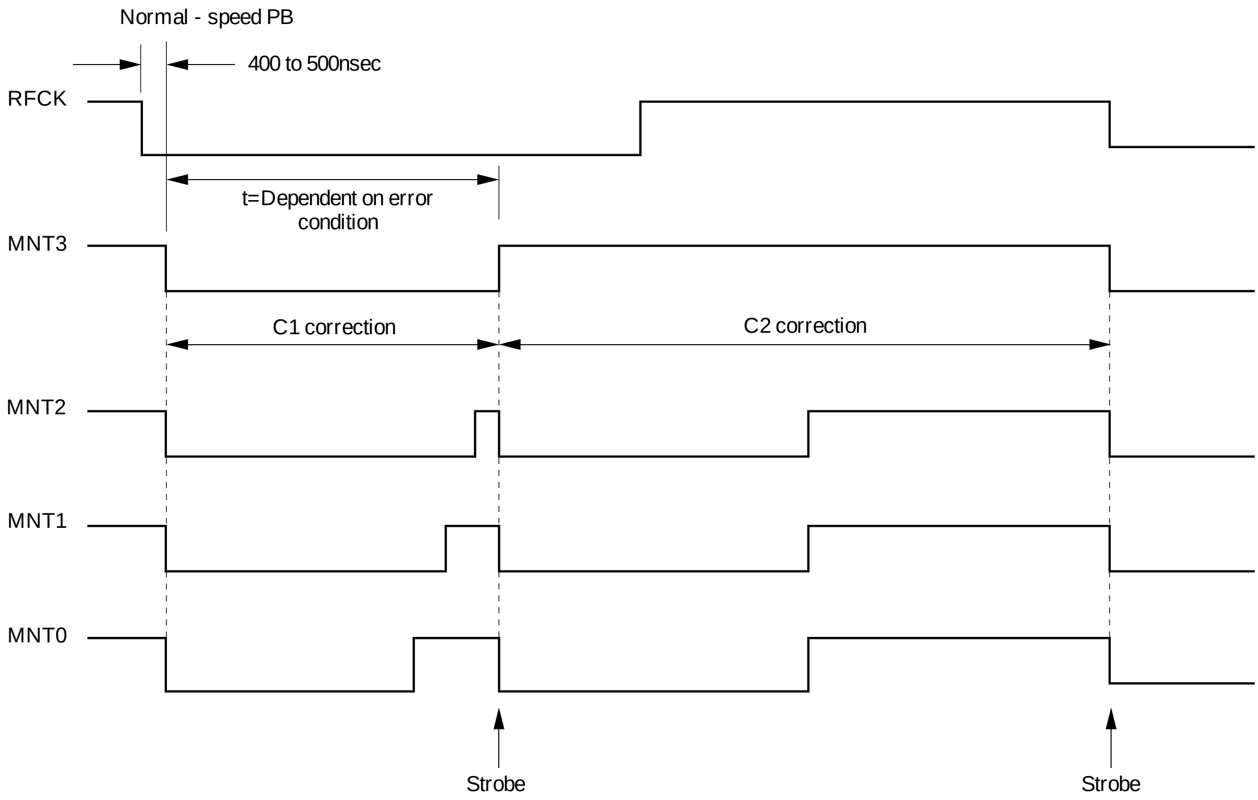
§3-3 Error Correction

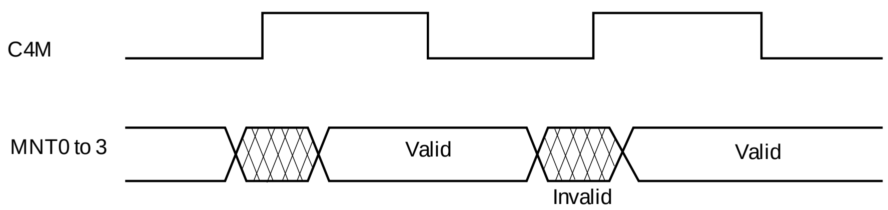
- On CDs, each data unit (8 bits) is formatted so that it is contained in two correction codes, C1 and C2. C1 consists of 28 bytes of information and 4-byte parity, whereas C2 is made up of 24 bytes of information and 4-byte parity. Both C1 and C2 comprise a read Solomon code with a minimum distance of 5.
- C1 realizes double corrections and C2 realizes quadruple corrections, both by the refined superstrategy method.
- To prevent erroneous C2 corrections, C1 pointer based on the conditions of C1 error, EFM signal play back, and player operation during C1 operation is attached to the corrected data.
- The status of error correction can be monitored from outside the LSI. It is indicated as shown in Table 3-2.
- When C2 pointer is High, this signifies uncorrectable data error. The data are either previous data held subsitute the error, or an average value interpolation.

MNT3	MNT2	MNT1	MNT0	Description
0	0	0	0	C1: No error detected. C1 pointer reset.
0	0	0	1	C1: 1 error corrected. C1 pointer set.
0	0	1	0	—
0	0	1	1	—
0	1	0	0	C1: No error detected. C1 pointer set.
0	1	0	1	C1: 1 error corrected. C1 pointer set.
0	1	1	0	C1: 2 errors corrected. C1 pointer set.
0	1	1	1	C1: Uncorrectable error. C1 pointer set.
1	0	0	0	C2: No error detected. C2 pointer reset.
1	0	0	1	C2: 1 error corrected. C2 pointer reset.
1	0	1	0	C2: 2 errors corrected. C2 pointer reset.
1	0	1	1	C2: 3 errors corrected. C2 pointer reset.
1	1	0	0	C2: 4 errors corrected. C2 pointer reset.
1	1	0	1	—
1	1	1	0	C2: Uncorrectable error. C1 pointer copied.
1	1	1	1	C2: Uncorrectable error. C2 pointer set.

Table 3-2 Indication of error correction status

Timing Chart 3-3





§3-4 DA Interface

- The CXD2500B has two modes of DA interface.

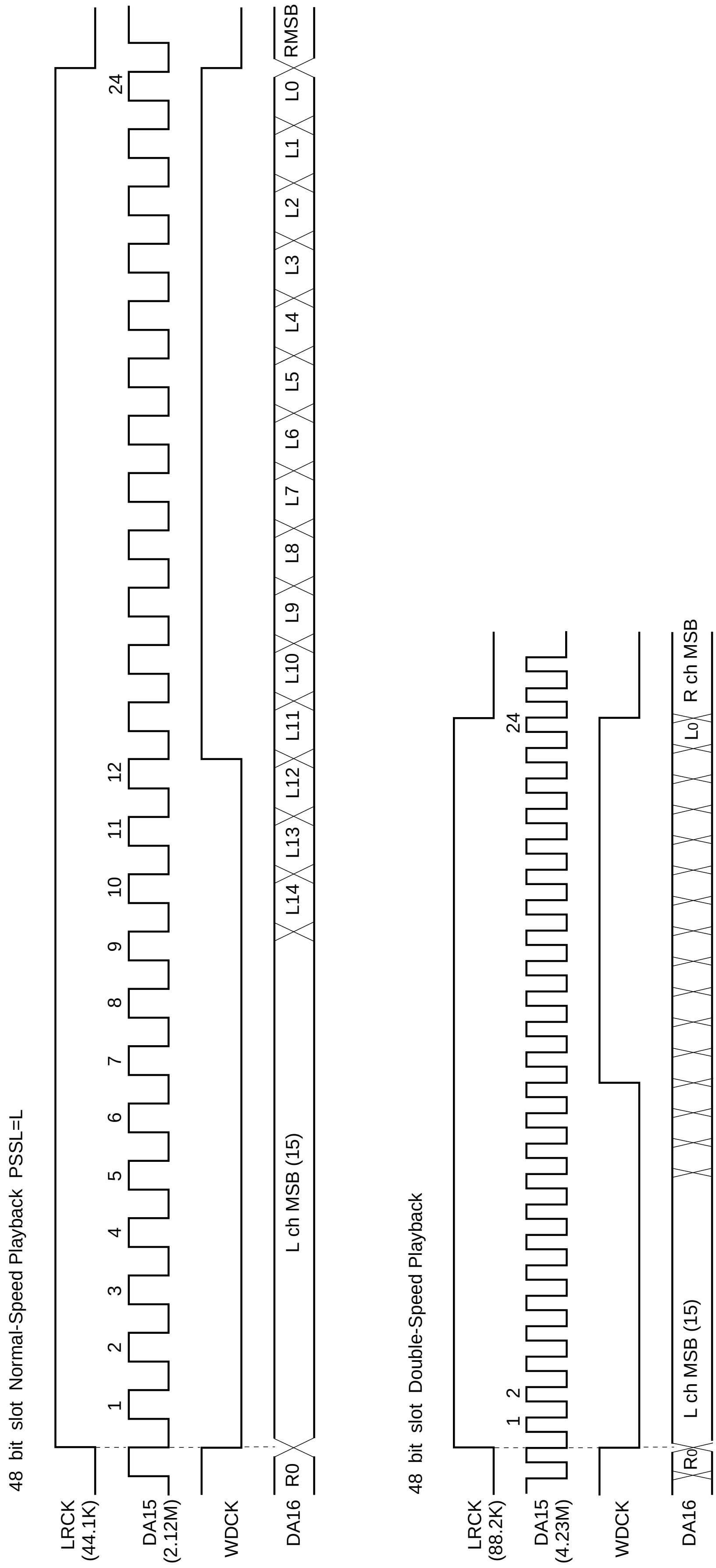
  a) 48-bit slot interface

  This is an MSB-first interface made up of LRCK signals with 48-bit clock cycles per LRCK cycle. While the LRCK signal is High, the data going through this interface is of the left channel.

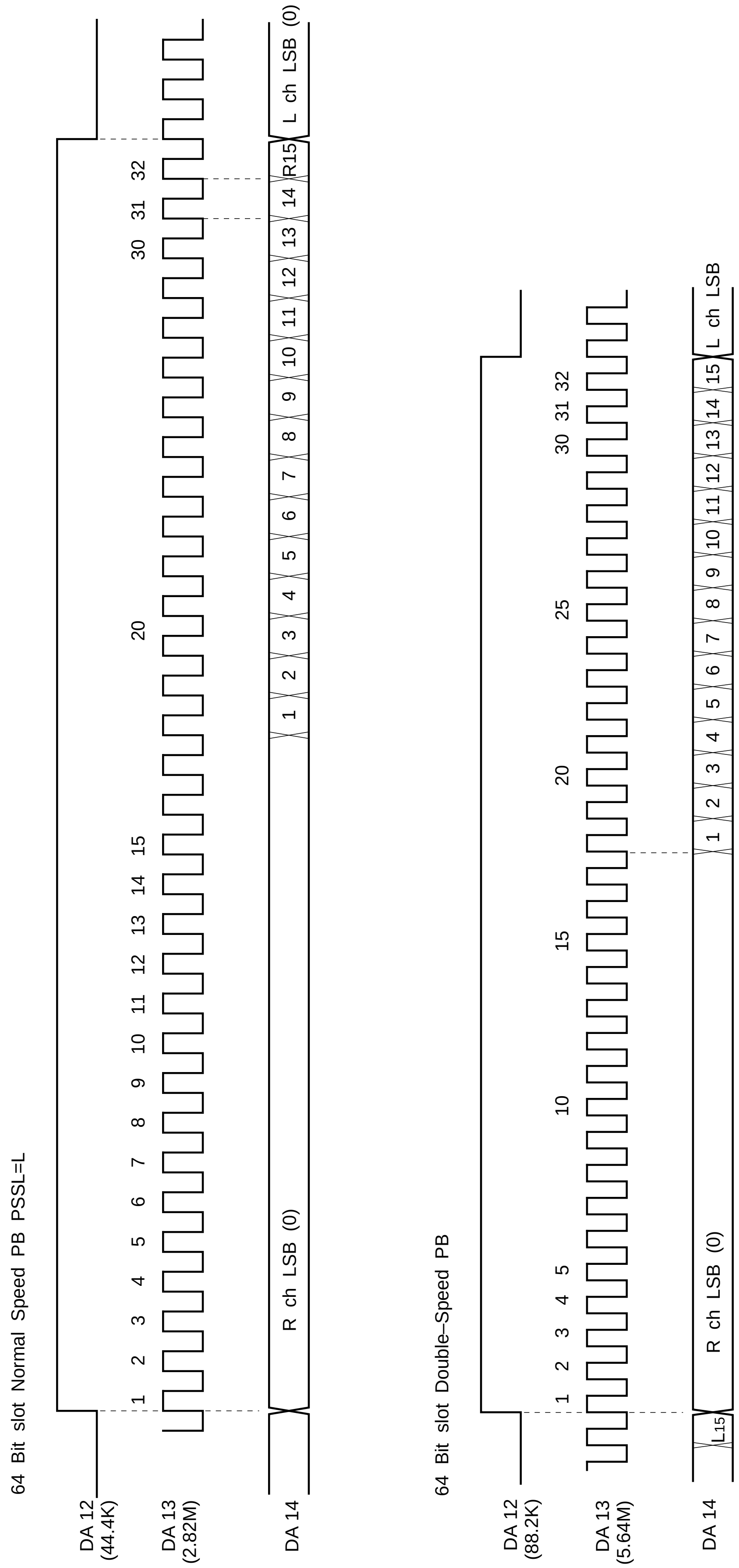
  b) 64-bit slot interface

  This is an LSB-first interface made up of LRCK signals with 64-bit clock cycles per LRCK cycle. While the LRCK signal is Low, the data going through this interface is of the left channel.

Timing Chart 3-4



Timing Chart 3-5



§3-5 Digital Out

There are three digital-out formats: type 1 for use at broadcasting stations, type 2, form 1 for use in general civil applications, and type 2, form 2 for use in software production. The CXD2500B supports type 2, form 1.

The clock accuracy for the channel status is automatically set at Level II when the X'tal clock is used, or Level III when vari-pitch control is made.

CRC checks are conducted on the Sub-Q data on the first 4 bits (bits 0-3). The data is input only after two checks are passed in succession.

The X'tal clock is set to 34 MHz, and variable pitch is reset. When D out is output at DSPB=1, set MD2 to 0 and turn off D out 34.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub-Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32	0															
48																
176																

Bits 0-3: Sub-Q control bits required to pass the CRC twice in succession.

bit 29: Varipitch: 1 X'tal: 0

Table 3-6 Digital Out C bits

§3-6 Servo Auto Sequencer

The servo auto sequencer controls a series of operation including auto-focusing and track jumping. When an auto sequence command is received from CPU, the servo auto sequencer automatically executes auto-focusing, 1-track jumping, 2N track jumping and M track moving.

During auto sequence execution (X Busy=Low), as SSP (servo signal processing LSI) is used exclusively, commands from CPU are not transferred to SSP. Instead, the commands can be sent to CXD2500B.

To make this servo auto sequencer usable, connect a CPU, RF and SSP to the CXD2500B as shown in Figure 3-7 and set A.SEQ ON-OFF of Register 9 to ON.

When the CLOK changes from Low to High while XBUSY is at Low, from that point on to a maximum of 100 µsec, X BUSY does not become High.

Due to the monostable multivibrator which is reset when CLOK is Low (XBUSY=Low), transfer of erroneous data to SSP is prevented when XBUSY changes from Low to High.

(a) Auto Focus ($47)

In auto focus operation, 'focus search up' is performed, FOK and FZC are checked, and the focus servo is turned on. When $47 is received from CPU, the focus servo is turned on through the steps shown in Figure 3-8. Since this auto focus sequence begins with 'focus search up,' it requires the pickup to be put down (focus search down) beforehand.

Blind E of Register 5 is used to eliminate chattering from FZC. The focus servo is turned on at the trailing edge of FZC after staying High continuously for a longer period than E.

System Configuration for Auto Sequencer Operation (Example)

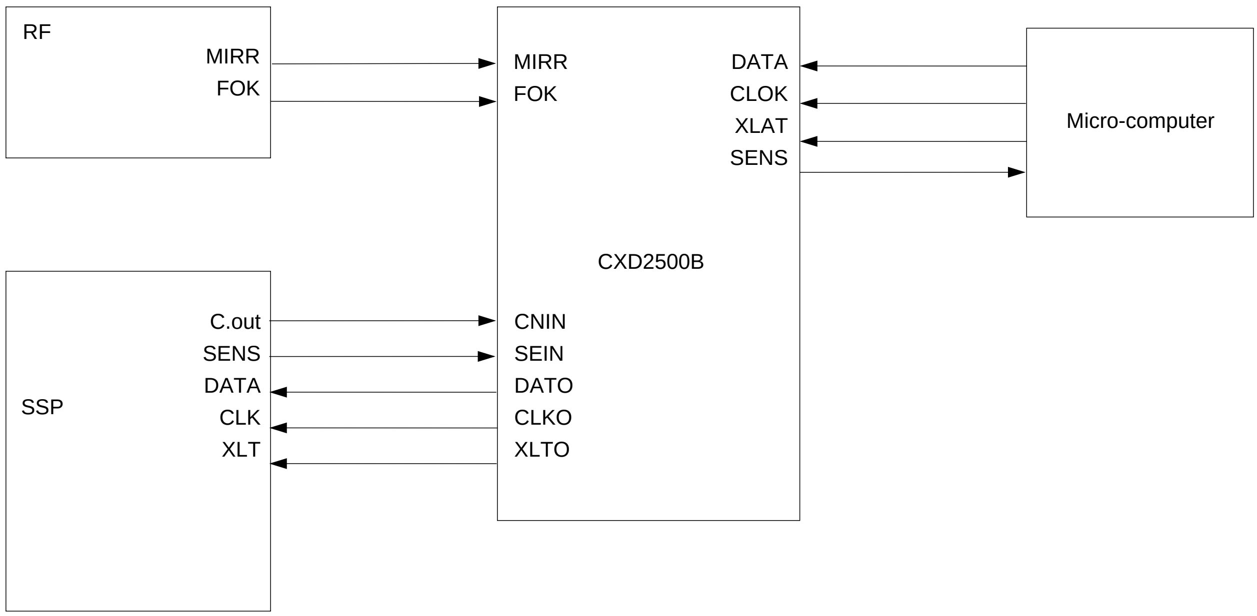


Figure 3-7

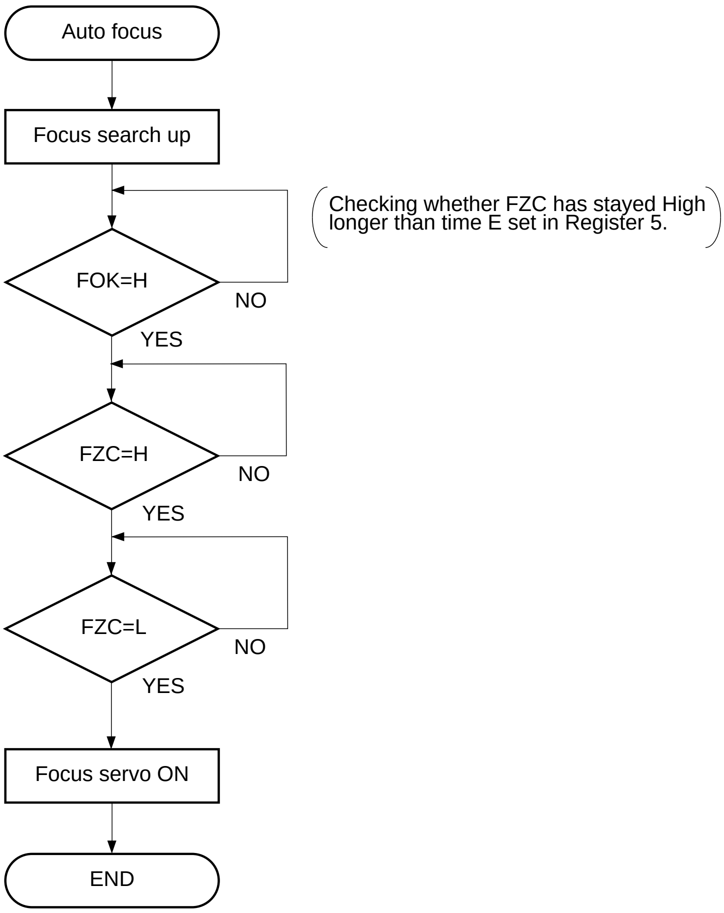


Figure 3-8 (a) Flow chart of auto focus operation

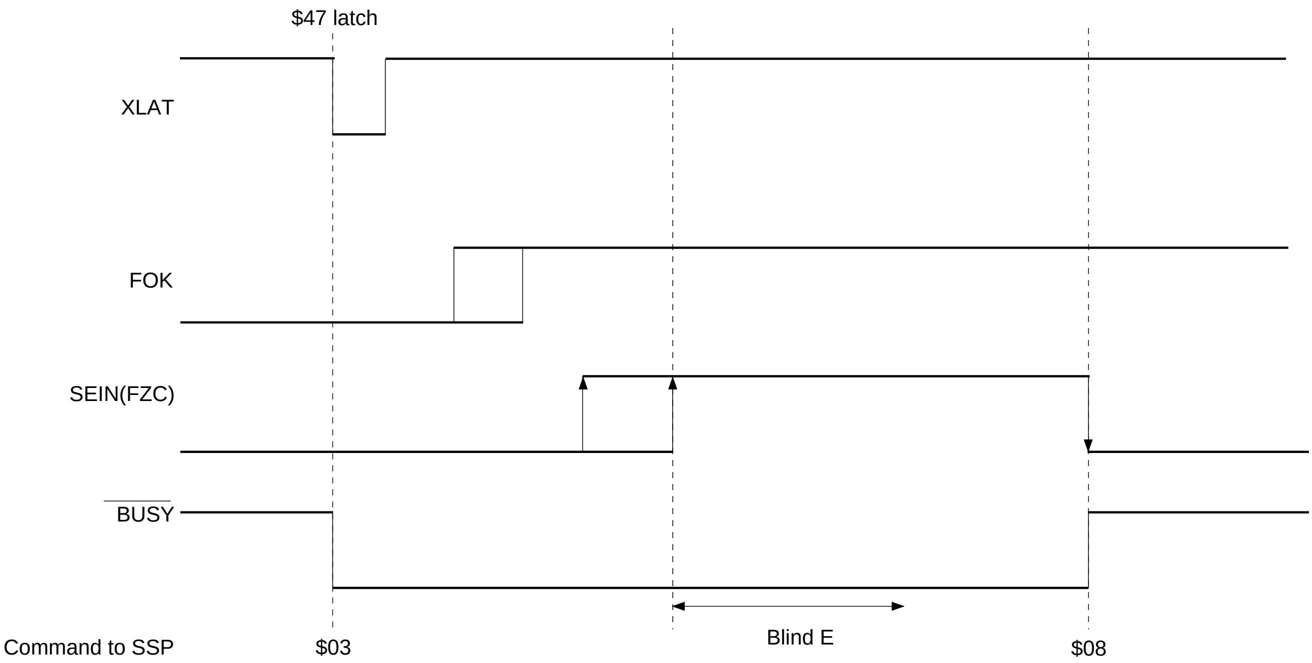


Figure 3-8 (b) Timing chart for auto focus operation

(b) Track Jump

Track jump operation includes 1, 10 and 2N track jumps. Do not perform this track jump unless the focus, tracking and sled servos are on. Such steps as tracking gain up and braking are not included in this track jump. Therefore, the commands for tracking gain up and brake ON ($17) must be issued in advance.

- 1-track jump

  When a $48 is received from CPU (or a $49 from REV), the servo auto sequencer executes a FWD (REV) 1-track jump as shown Figure 3-9. The values of blind A and brake B must be set in Register 5.

- 10-track jump

  When a $4H is received from CPU (or a $4B from REV), the servo auto sequencer executes a FWD (REV) 10-track jump as shown in Figure 3-10. The principal difference between the 1-track and 10-track jumps is whether the sled is kicked or not. In the 10-track jump, the actuator after being kicked is braked when CNIN has been counted 5 tracks. When the actuator has adequately slowed down as a result of braking, the tracking and sled servos are turned on (this actuator slow-down is detected by checking whether the CNIN period has exceeded overflow C specified in Register 5).

- 2N track jump

  When a $4C is received from CPU (or a $4D from REV), the servo auto sequencer executes a FWD (REV) 2N track jump. The number of tracks to be jumped is determined by N, set Register 7 beforehand. The maximum permissible number is 2^{16}. In actual use, however, it is subject to limitation imposed by the actuator.

  When N is smaller than 16, the jumps are counted by means of counting CNIN signals. If N is 16 and above, MIRR signals are counted instead of CNIN signals.

  The 2N track jump sequence is basically the same as the 10-track jump sequence. The only difference between them is that, in the 2N track jump sequence, the sled is kept moving for time D specified in Register 6 after the tracking servo is turned on.

- M track move

  When a $4E is received from CPU (or a $4F from REV), the servo auto sequencer executes a FWD (REV) M-track move as shown in Figure 3-12. The maximum value that can be set from M is 2^{16}. The track moves are counted in the same way as for 2N track jumps. That is, when M is smaller than 16, the moves are counted by means of counting CNIN signals. If M is 16 and above, MIRR signals are counted instead of the CNIN signals. In this M track move, only the sled is moved. This method is suitable for a large track move ranging from several thousand to several tens of thousand tracks.

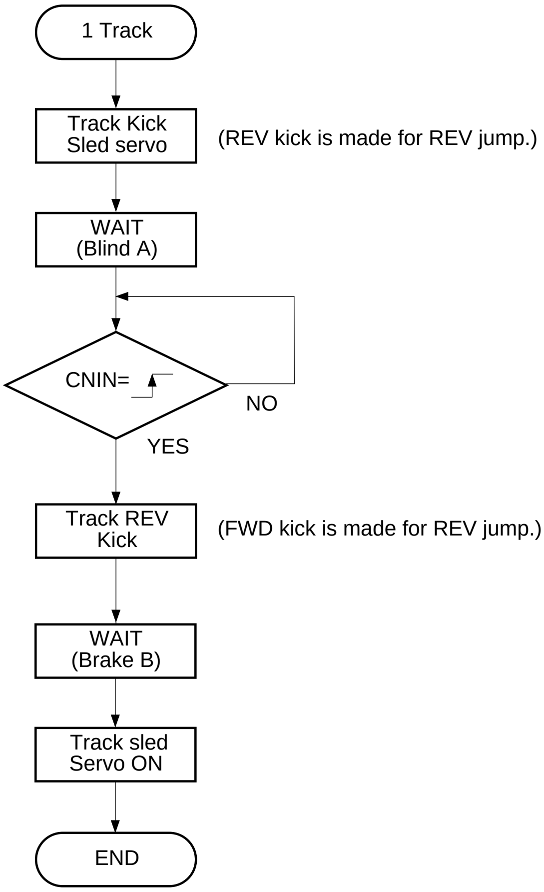


Figure 3-9 (a) Flow chart of 1-track jump

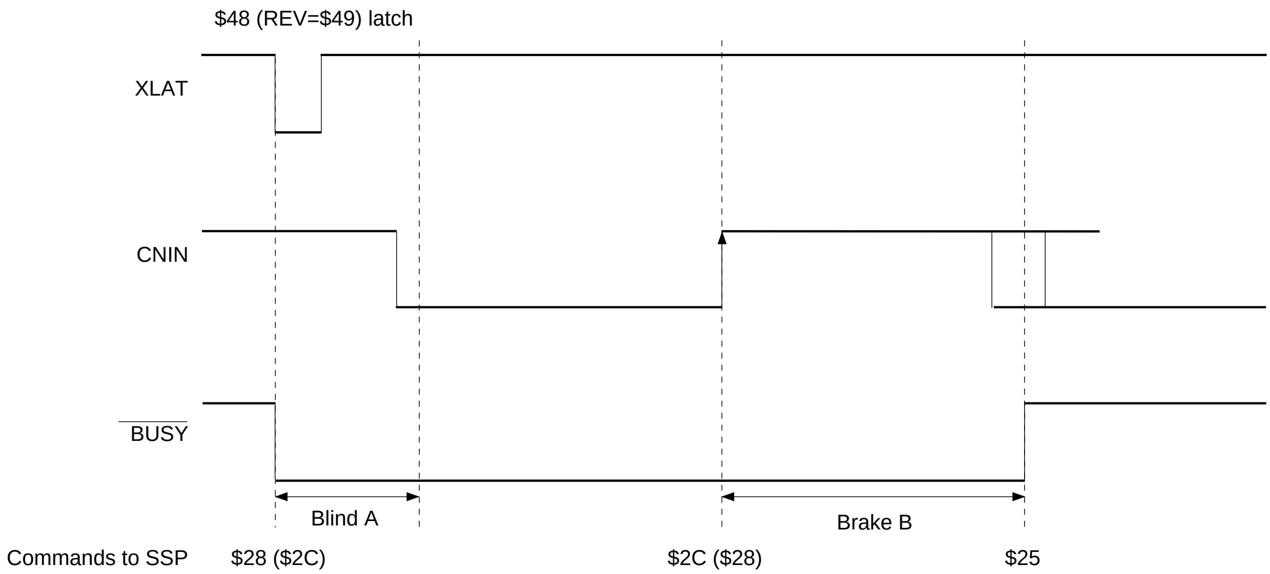


Figure 3-9 (b) Timing chart for 1-track jump

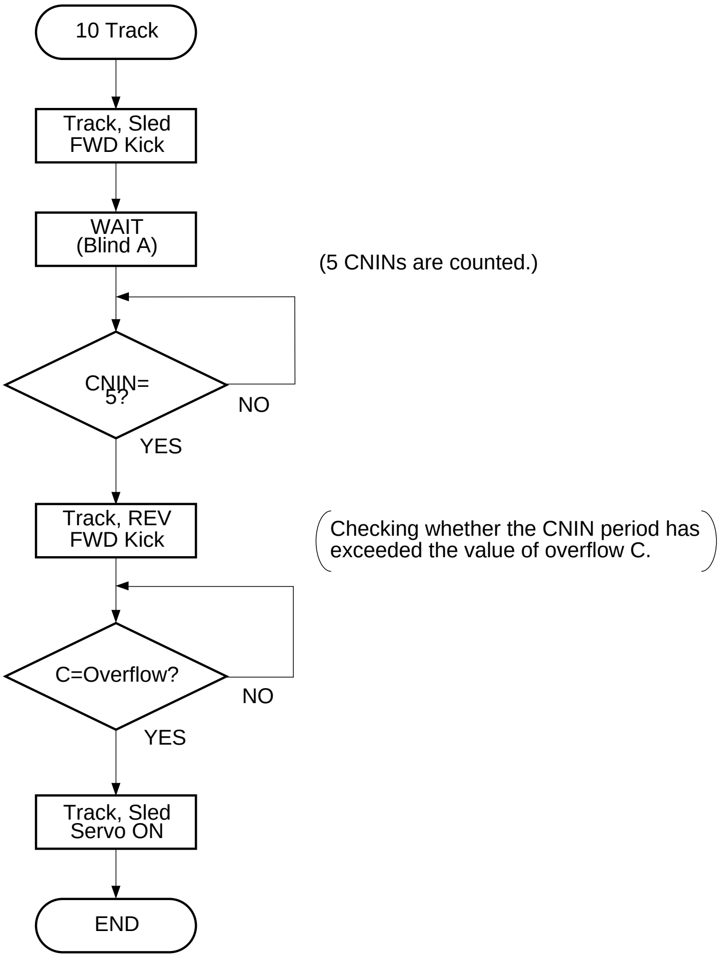


Figure 3-10 (a) Flow chart of 10-track jump

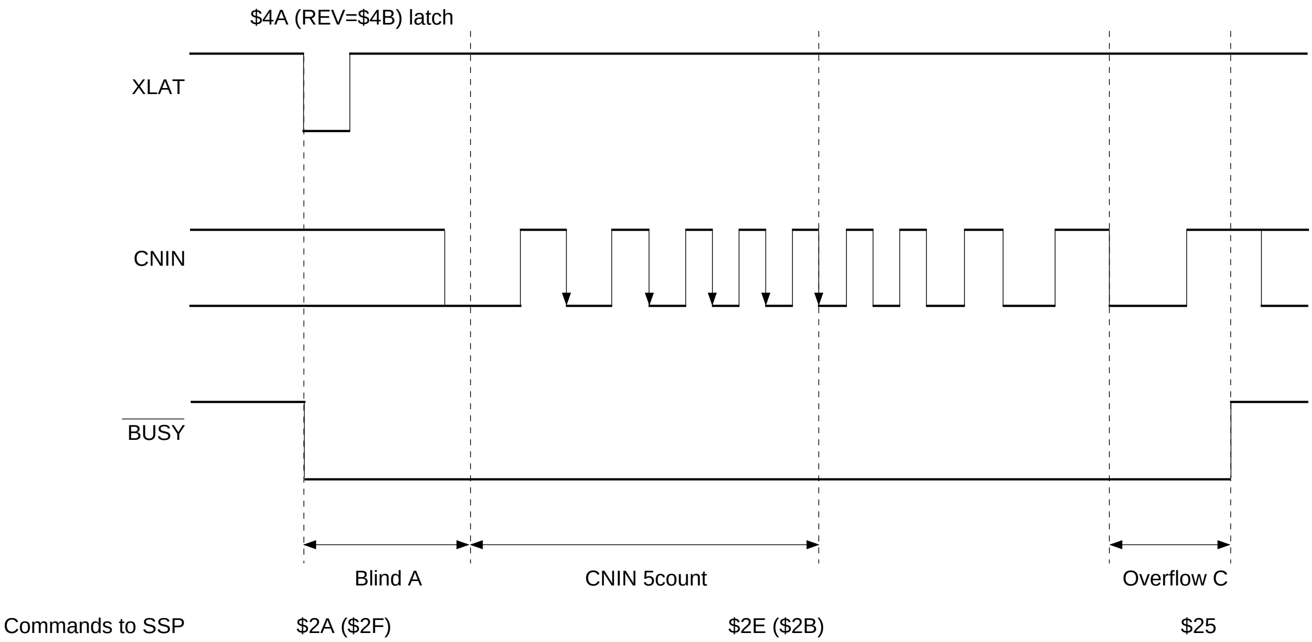


Figure 3-10 (b) Timing chart for 10-track jump

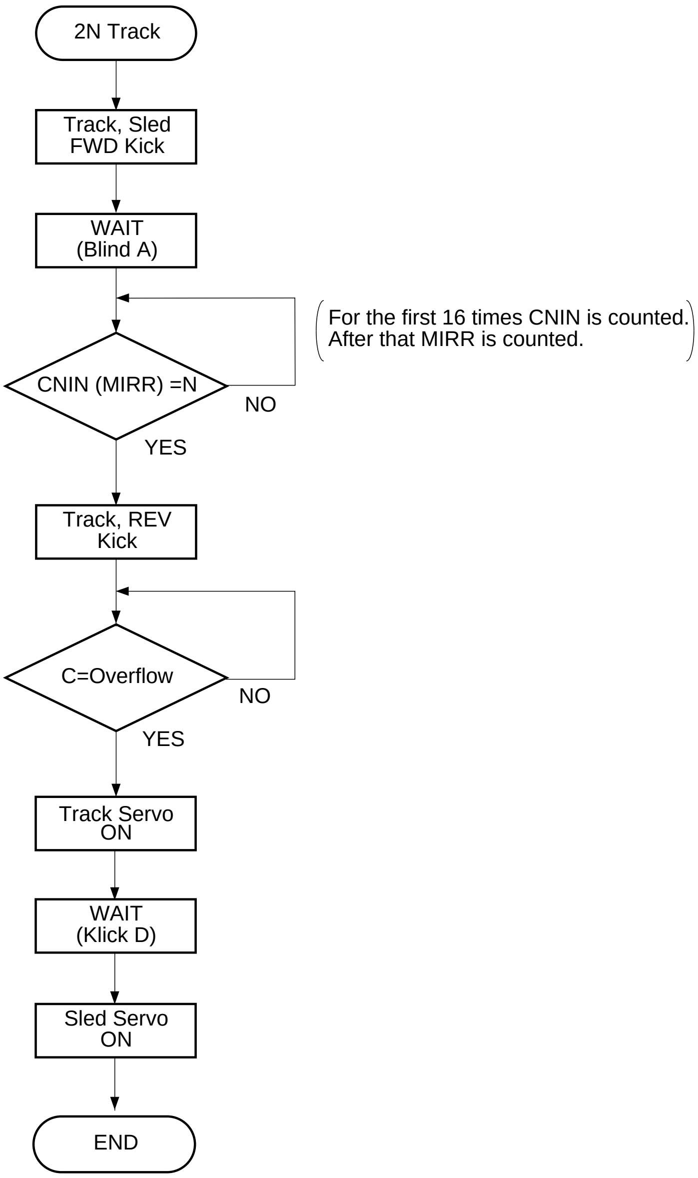


Figure 3-11 (a) Flow chart of 2N track jump

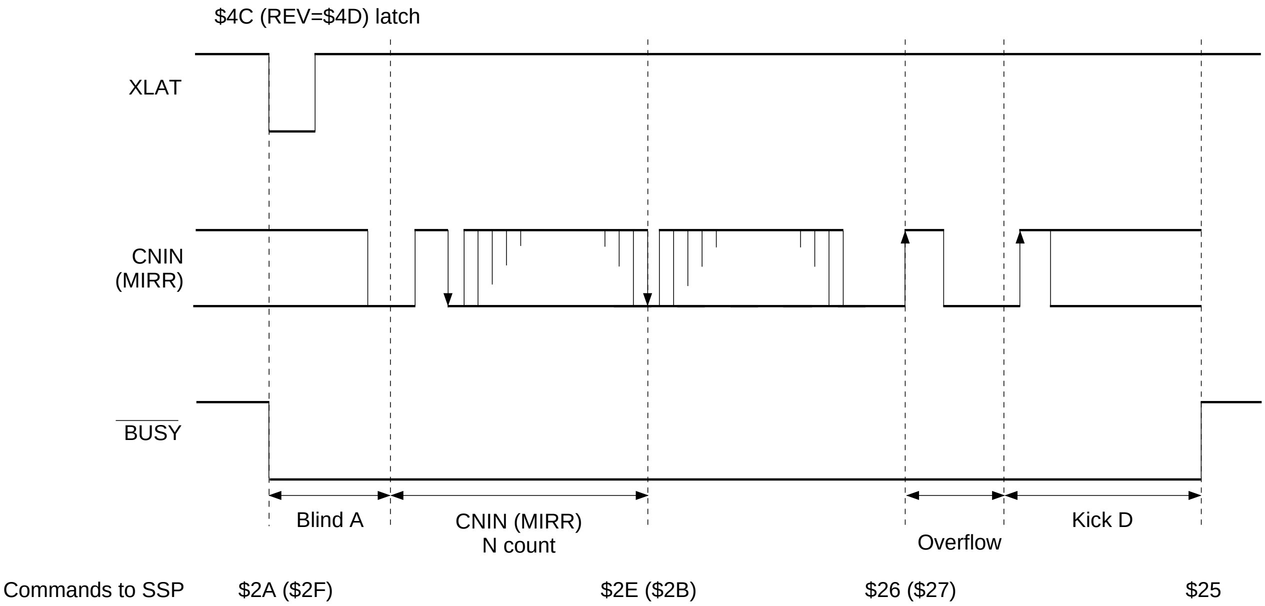


Figure 3-11 (b) Timing chart for 2N track jump

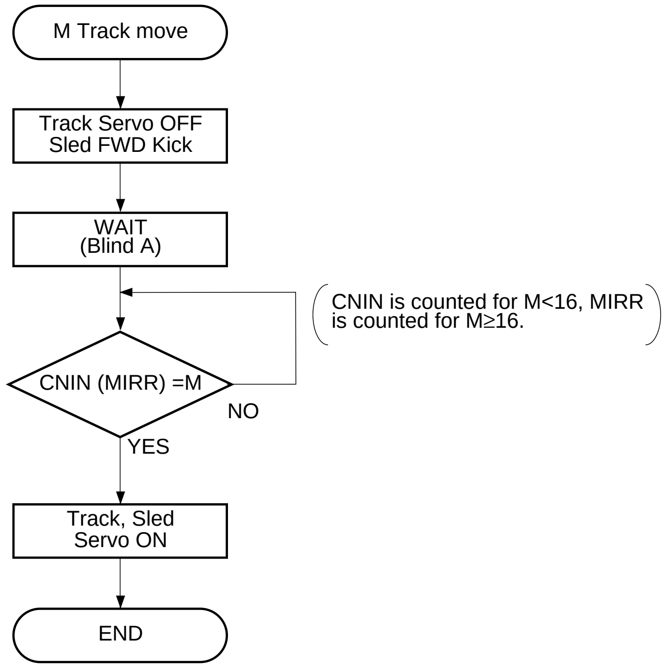


Figure 3-12 (a) Flow chart of M track move

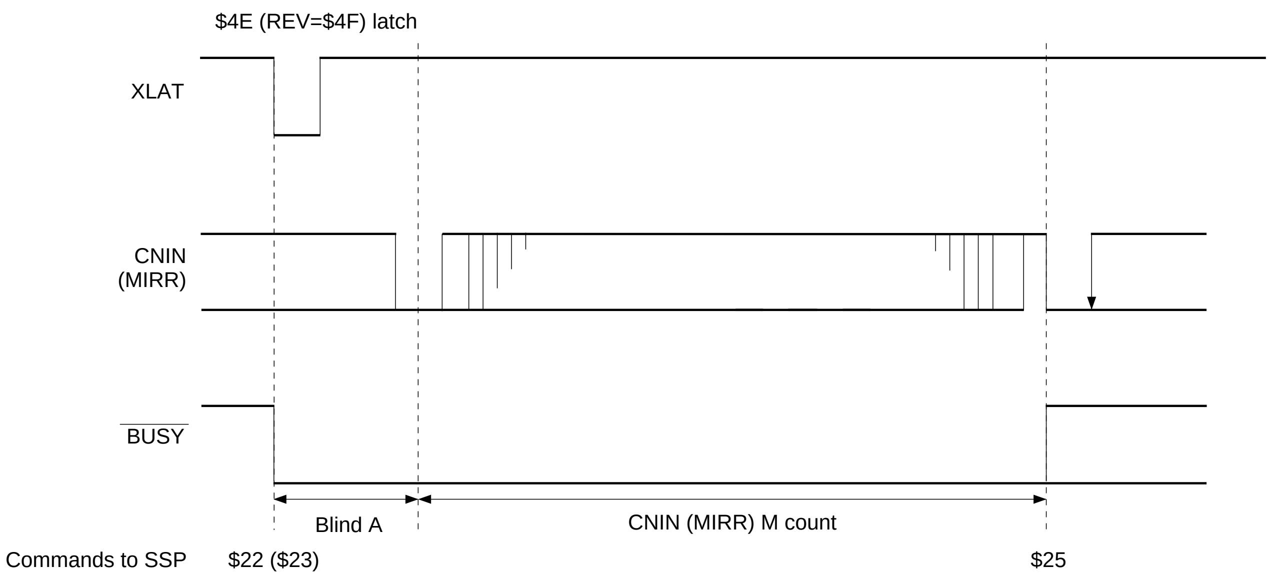


Figure 3-12 (b) Timing chart for M track move

§3-7 Digital CLV

The digital CLV is a digital spindle servo, of which its block diagram is shown in Figure 3-14. It is capable of outputting MDS or MDP error signals by the PWM method after raising the sampling frequency up to 130 kHz based on the normal speed in the CLVS, CLVP and other modes. It also permits gain setting.

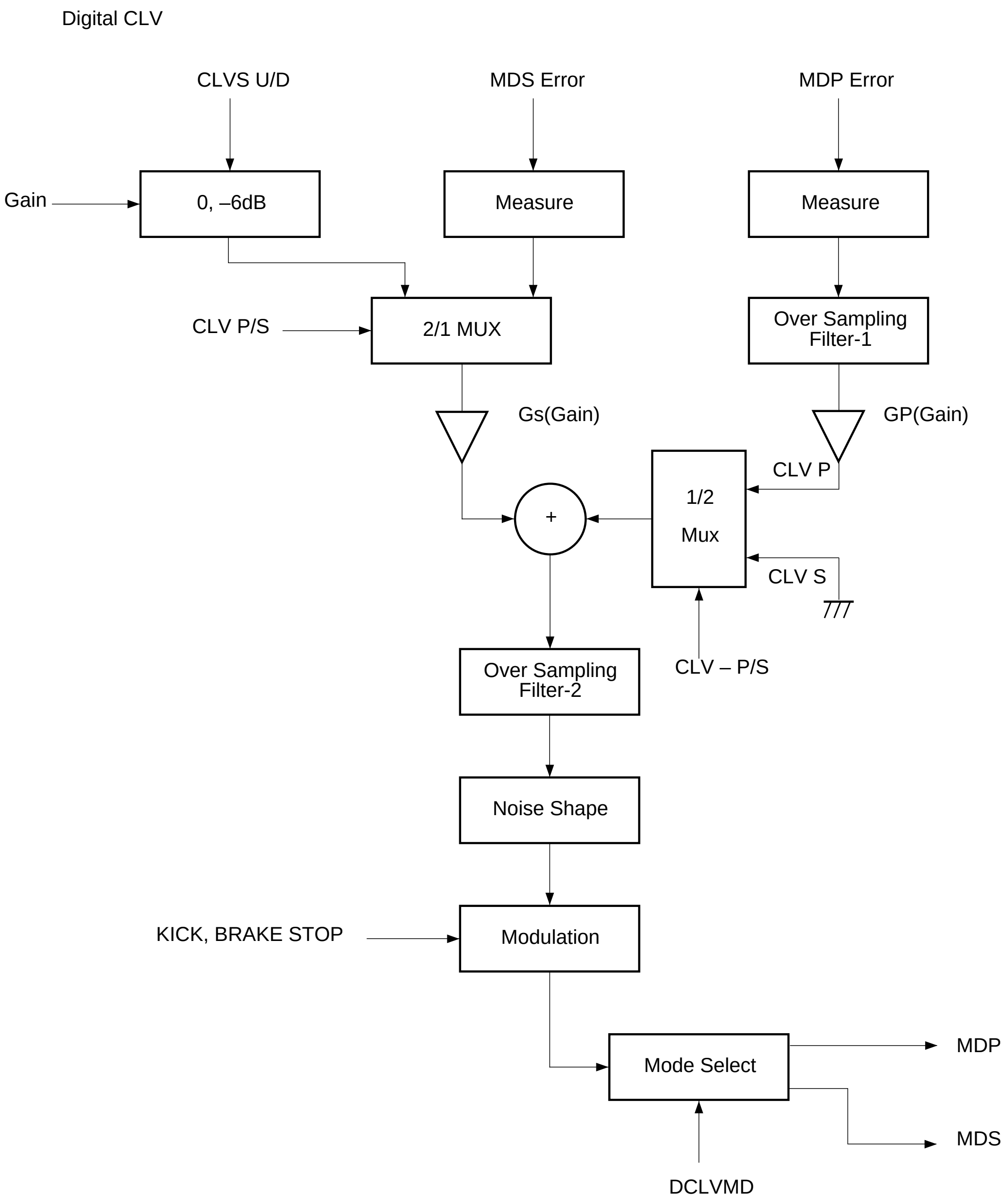


Figure 3-14 Block diagram

§3-8 Asymmetry correction

Block diagram and circuit example are shown on Fig. 3-15.

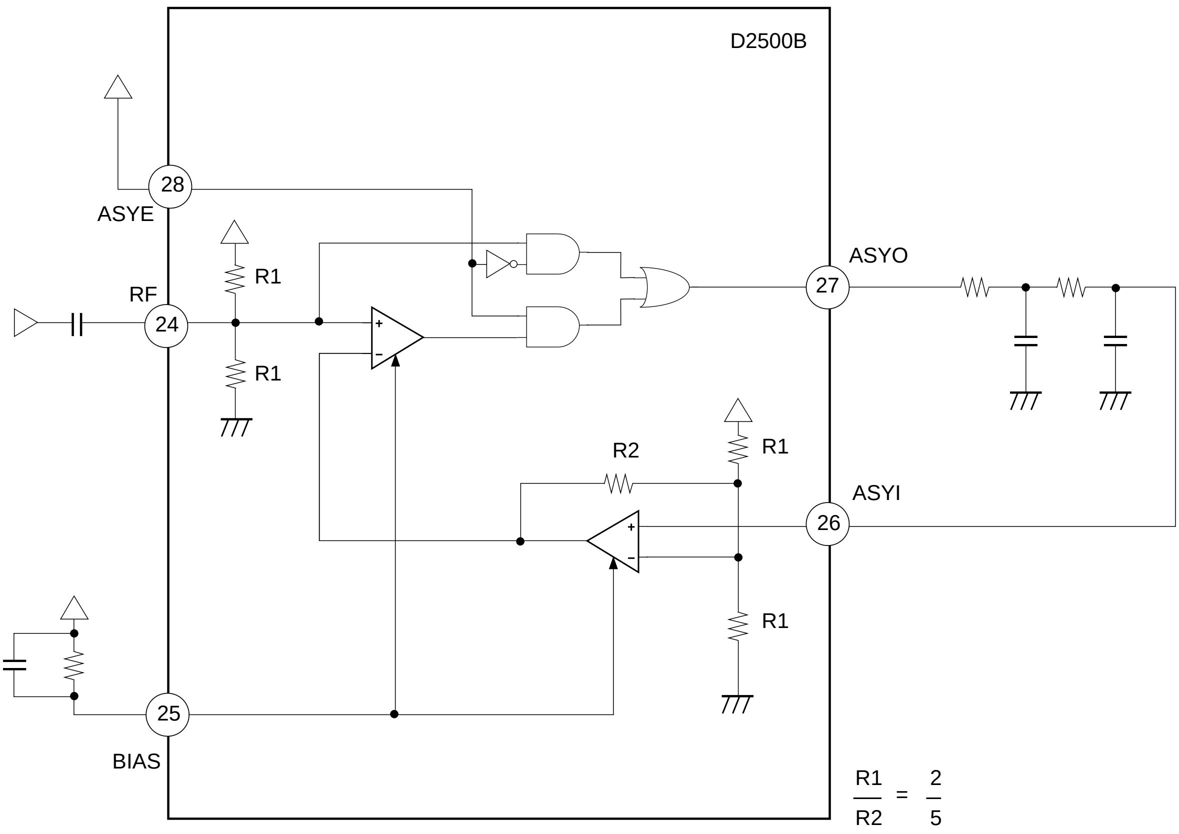
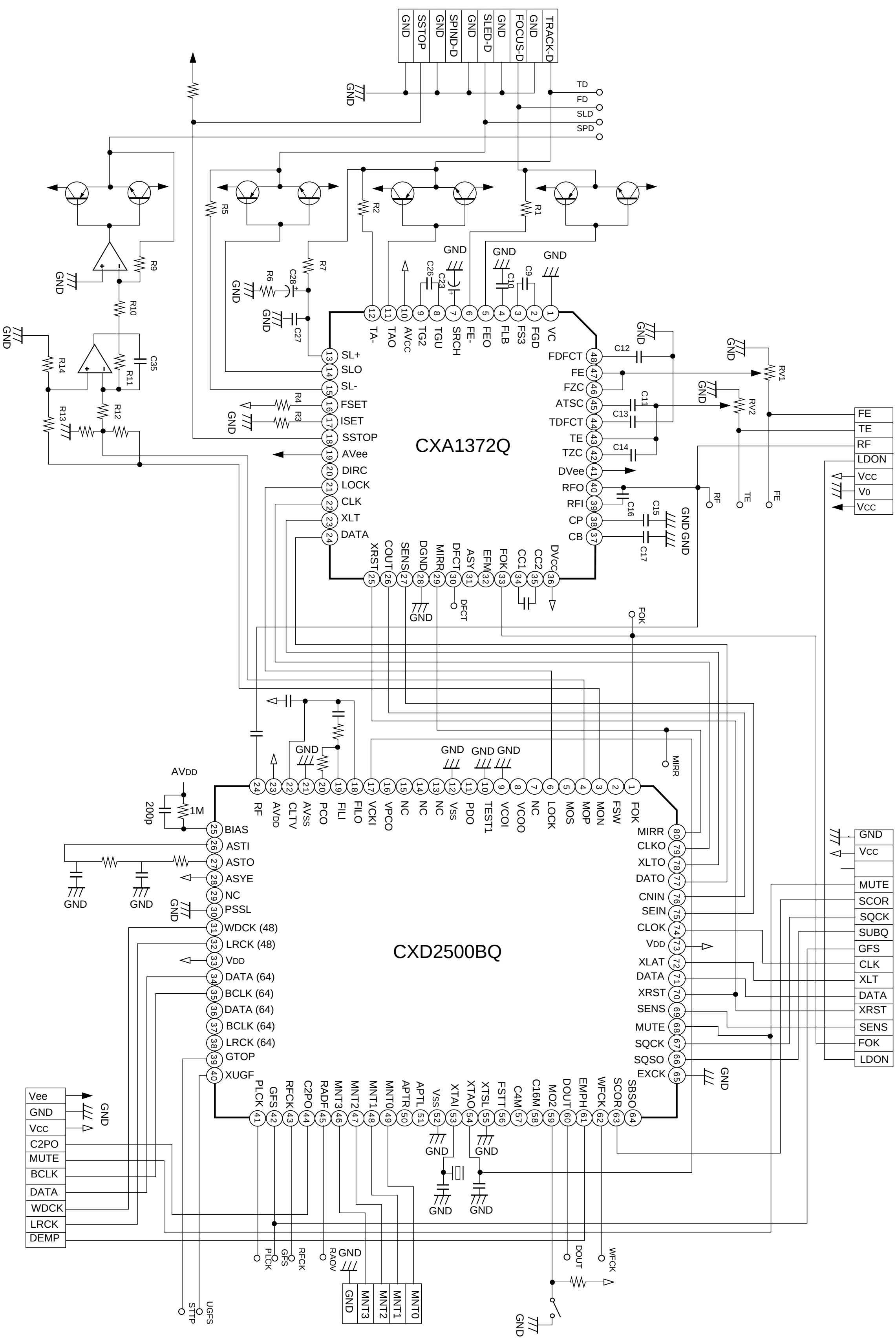


Figure 3-15 Asymmetry correction application circuit example

Application Circuit

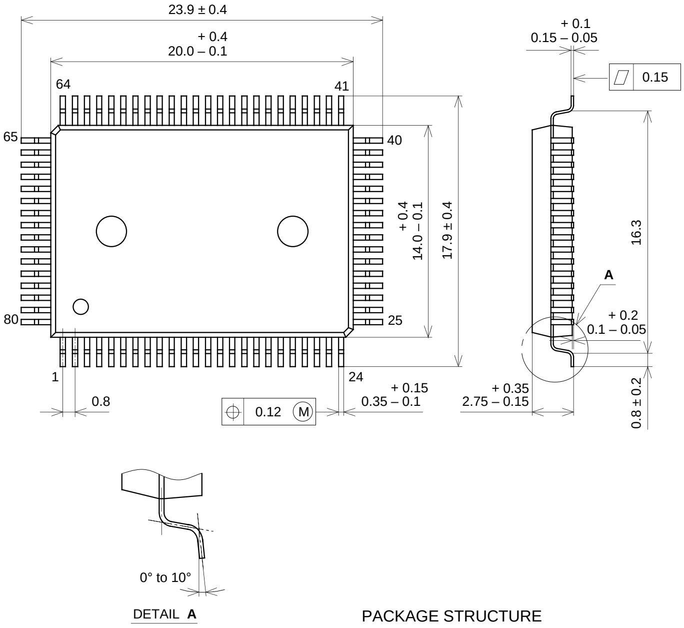


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Package Outline   Unit : mm

CXD2500BQ

80PIN QFP (PLASTIC)



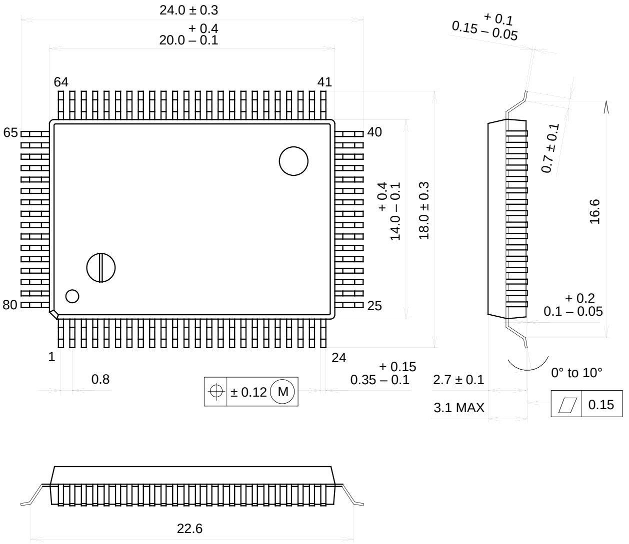
PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	——————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g

CXD2500BQ

80PIN QFP (PLASTIC)



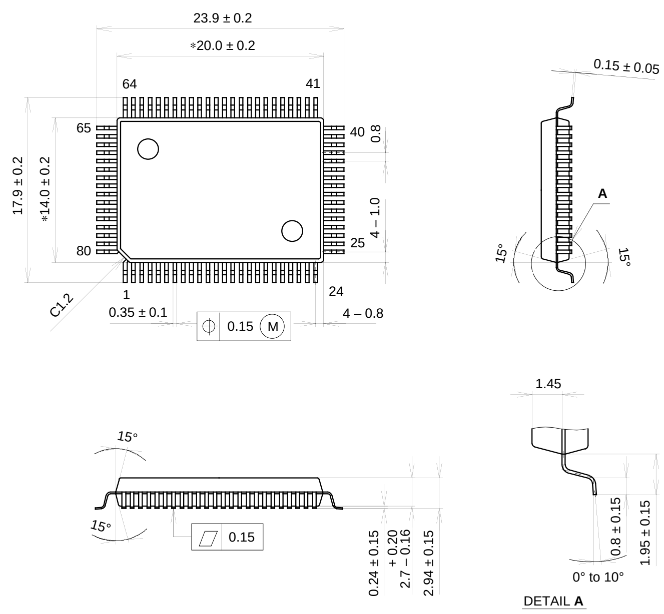
PACKAGE STRUCTURE

SONY CODE	QFP-80P-L121
EIAJ CODE	*QFP080-P-1420-AX
JEDEC CODE	——————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.6g

CXD2500BQ

QFP 80PIN (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	QFP-80P-L051
EIAJ CODE	∗QFP080-P-1420-AH
JEDEC CODE	——————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.6g